



80960JA/JF EMBEDDED 32-BIT MICROPROCESSOR

- High-Performance Embedded Architecture
 - One Instruction/Clock Execution
 - Load/Store Programming Model
 - Sixteen 32-Bit Global Registers
 - Sixteen 32-Bit Local Registers (8 sets)
 - Nine Addressing Modes
 - User/Supervisor Protection Model
- Two-Way Set Associative Instruction Cache
 - 80960JA - 2 KByte
 - 80960JF - 4 KByte
 - Programmable Cache Locking Mechanism
- Direct Mapped Data Cache
 - 80960JA - 1 KByte
 - 80960JF - 2 KByte
 - Write Through Operation
- On-Chip Stack Frame Cache
 - Seven Register Sets Can Be Saved
 - Automatic Allocation on Call/Return
 - 0-7 Frames Reserved for High-Priority Interrupts
- On-Chip Data RAM
 - 1 Kbyte Critical Variable Storage
 - Single-Cycle Access
- High Bandwidth Burst Bus
 - 32-Bit Multiplexed Address/Data
 - Programmable Memory Configuration
 - Selectable 8-, 16-, 32-Bit Bus Widths
 - Supports Unaligned Accesses
 - Big or Little Endian Byte Ordering
- New Instructions
 - Conditional Add, Subtract and Select
 - Processor Management
- High-Speed Interrupt Controller
 - 31 Programmable Priorities
 - Eight Maskable Pins plus NMI
 - Up to 240 Vectors in Expanded Mode
- Two On-Chip Timers
 - Independent 32-Bit Counting
 - Clock Prescaling by 1, 2, 4 or 8
 - Internal Interrupt Sources
- Halt Mode for Low Power
- IEEE 1149.1 (JTAG) Boundary Scan Compatibility
- Packages
 - 132-Lead Pin Grid Array (PGA)
 - 132-Lead Plastic Quad Flat-Pack (PQFP)

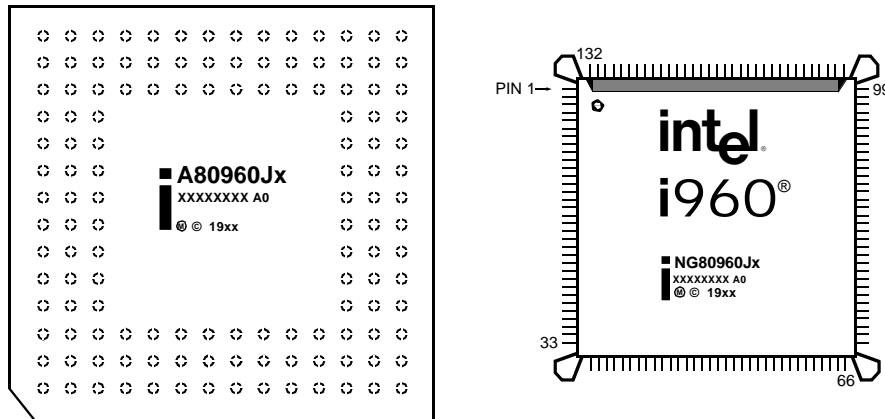


Figure 1. 80960JA/JF Microprocessors



**80960JA/JF
EMBEDDED 32-BIT MICROPROCESSOR**

1.0 PURPOSE 1

2.0 80960JA/JF OVERVIEW 1

 2.1 80960 Processor Core 2

 2.2 Burst Bus 2

 2.3 Timer Unit 3

 2.4 Priority Interrupt Controller 3

 2.5 Instruction Set Summary 3

 2.6 Faults and Debugging 3

 2.7 Low Power Operation 4

 2.8 Test Features 4

 2.9 Memory-Mapped Control Registers 4

 2.10 Data Types and Memory Addressing Modes 4

3.0 PACKAGE INFORMATION 6

 3.1 Pin Descriptions 6

 3.1.1 Functional Pin Definitions 6

 3.1.2 80960JA/JF 132-Lead PGA Pinout 12

 3.1.3 80960JA/JF PQFP Pinout 16

 3.2 Package Thermal Specifications 19

4.0 ELECTRICAL SPECIFICATIONS 21

 4.1 Absolute Maximum Ratings 21

 4.2 Operating Conditions 21

 4.3 Connection Recommendations 21

 4.4 DC Specifications 22

 4.5 AC Specifications 23

 4.5.1 AC Test Conditions and Derating Curves 25

 4.5.2 AC Timing Waveforms 27

5.0 BUS FUNCTIONAL WAVEFORMS 33

6.0 DEVICE IDENTIFICATION 45

7.0 REVISION HISTORY 45

CONTENTS



FIGURES

Figure 1	80960JA/JF Microprocessors	i
Figure 2	80960JA/JF Block Diagram	2
Figure 3	132-Lead Pin Grid Array Bottom View - Pins Facing Up	12
Figure 4	132-Lead Pin Grid Array Top View - Pins Facing Down	13
Figure 5	132-Lead PQFP - Top View	16
Figure 6	AC Test Load	25
Figure 7	Output Delay or Hold vs. Load Capacitance	26
Figure 8	Rise and Fall Time Derating	26
Figure 9	CLKIN Waveform	27
Figure 10	Output Delay Waveform for T_{OV1}	27
Figure 11	Output Float Waveform for T_{OF}	28
Figure 12	Input Setup and Hold Waveform for T_{IS1} and T_{IH1}	28
Figure 13	Input Setup and Hold Waveform for T_{IS2} and T_{IH2}	29
Figure 14	Input Setup and Hold Waveform for T_{IS3} and T_{IH3}	29
Figure 15	Input Setup and Hold Waveform for T_{IS4} and T_{IH4}	30
Figure 16	Relative Timings Waveform for T_{LXL} and T_{LXA}	30
Figure 17	DT/\overline{R} and \overline{DEN} Timings Waveform	31
Figure 18	TCK Waveform	31
Figure 19	Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}	32
Figure 20	Output Delay and Output Float for T_{BSOV1} AND T_{BSOF1}	32
Figure 21	Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}	33
Figure 22	Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}	33
Figure 23	Non-Burst Read and Write Transactions Without Wait States, 32-Bit Bus	34
Figure 24	Burst Read and Write Transactions Without Wait States, 32-Bit Bus	35
Figure 25	Burst Write Transactions With 2,1,1,1 Wait States, 32-Bit Bus	36
Figure 26	Burst Read and Write Transactions Without Wait States, 8-Bit Bus	37
Figure 27	Burst Read and Write Transactions With 1, 0 Wait States and Extra T_r State on Read, 16-Bit Bus	38
Figure 28	Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit Bus, Little Endian	39
Figure 29	HOLD/HOLDA Waveform For Bus Arbitration	40
Figure 30	Summary of Aligned and Unaligned Accesses (32-Bit Bus)	42
Figure 31	Summary of Aligned and Unaligned Accesses (32-Bit Bus) (Continued)	43
Figure 32	Cold Reset Waveform	44



TABLES

Table 1	80960JA/JF Instruction Set	5
Table 2	Pin Description Nomenclature	6
Table 3	Pin Description — External Bus Signals	7
Table 4	Pin Description — Processor Control Signals, Test Signals and Power	10
Table 5	Pin Description — Interrupt Unit Signals	11
Table 6	132-Lead PGA Pinout — In Signal Order	14
Table 7	132-Lead PGA Pinout — In Pin Order	15
Table 8	132-Lead PQFP Pinout — In Signal Order	17
Table 9	132-Lead PQFP Pinout — In Pin Order	18
Table 10	132-Lead PGA Package Thermal Characteristics	19
Table 11	132-Lead PQFP Package Thermal Characteristics	20
Table 12	Targeted 80960JA/JF Operating Conditions	21
Table 13	Targeted 80960JA/JF DC Characteristics	22
Table 14	Targeted 80960JA/JF Input Clock Timings	23
Table 15	Targeted 80960JA/JF Synchronous Output Timings	24
Table 16	Targeted 80960JA/JF Synchronous Input Timings	24
Table 17	Targeted 80960JA/JF Relative Output Timings	24
Table 18	Targeted 80960JA/JF Boundary Scan Test Signal Timings	25
Table 19	Natural Boundaries for Load and Store Accesses	40
Table 20	Summary of Byte Load and Store Accesses	41
Table 21	Summary of Short Word Load and Store Accesses	41
Table 22	Summary of n-Word Load and Store Accesses (n = 1, 2, 3, 4)	41
Table 23	80960JA/JF Die and Stepping Reference	45
Table 24	Data Sheet Version -002 to -003 Revision History	45
Table 25	Data Sheet Version -001 to -002 Revision History	46

CONTENTS



v

ADVANCE INFORMATION



1.0 PURPOSE

This document provides advance information for the 80960JA/JF microprocessor, including targeted electrical characteristics and package pinout information. Detailed functional descriptions — other than parametric performance — are published in the *i960® Jx Microprocessor User's Manual (272483)*.

2.0 80960JA/JF OVERVIEW

The 80960JA/JF, a new member in the family of embedded i960® processors, provides high performance to cost-sensitive 32-bit embedded applications. The 80960JA/JF is object code compatible with the 80960 Core Architecture and is capable of sustained execution at the rate of one instruction per clock. This processor's features include generous instruction cache, data cache and data RAM. It also boasts a fast interrupt mechanism, dual programmable timer units and new instructions.

Memory subsystems for cost-sensitive embedded applications often impose substantial wait state penalties. The 80960JA/JF integrates considerable storage resources on-chip to decouple CPU execution from the external bus.

The 80960JF includes a 4 Kbyte instruction cache and a 2 Kbyte data cache. For greater economy, the 80960JA includes a 2 Kbyte instruction cache and a 1 Kbyte data cache. Both processors include a 1 Kbyte data RAM.

The 80960JA/JF rapidly allocates and deallocates local register sets during context switches. The processor needs to flush a register set to the stack only when it saves more than seven sets to its local register cache.

A 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals simplifies the connection of the 80960JA/JF to external components. The user programs physical and logical memory attributes through memory-mapped control registers (MMRs) — an extension not found on the i960 Kx, Sx or Cx processors. Physical and logical configuration registers enable the processor to operate with all combinations of bus width and data object alignment. The processor supports a homogeneous byte ordering model.

This processor integrates two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers, an extension to the familiar 80960 architecture.

The Timer Unit offers two independent 32-bit timers for use as real-time system clocks and general purpose system timing. These operate in either single-shot or auto-reload mode and can generate interrupts.

The interrupt controller unit (ICU) provides a flexible, low-latency means for requesting interrupts. It provides full programmability of up to 240 interrupt sources into 31 priority levels. The ICU takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. Local registers may be dedicated to high-priority interrupts to further reduce their latency. Acting independently from the core, the ICU compares the priorities of posted interrupts with the current process priority, off-loading this task from the core. The ICU also supports the integrated timer interrupts.

The 80960JA/JF features a Halt mode designed to support applications where low power consumption is critical. The **halt** instruction lets you shut down instruction execution, resulting in a power savings of up to 90 percent.

The 80960JA/JF's testability features, including ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

The *Solutions960®* program features a wide variety of development tools that support the i960 processor family. Many of these tools are developed by partner companies; some are developed by Intel, such as profile-driven optimizing compilers. For more information on these products, contact your local Intel representative.

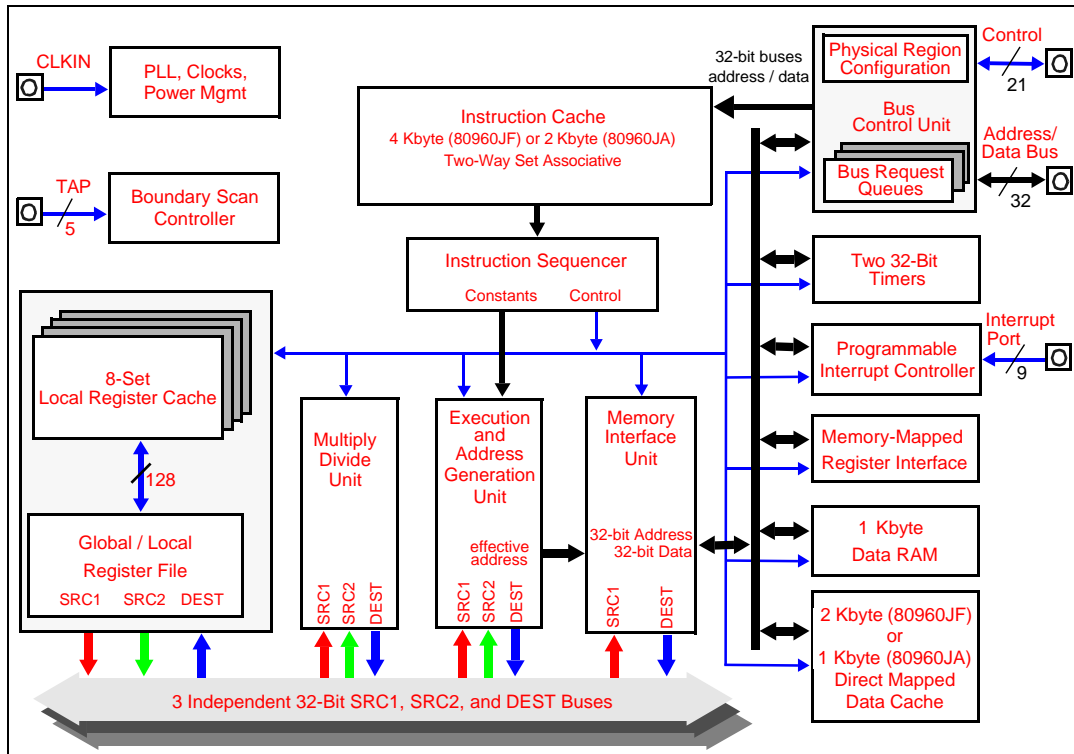


Figure 2. 80960JA/JF Block Diagram

2.1 80960 Processor Core

The 80960JA/JF microprocessor is a new, scalar implementation of the 80960 Core Architecture. Intel designed it to be a very high performance device that is also cost-effective. Factors that contribute to the core's performance include:

- Single-clock execution of most instructions
- Independent Multiply/Divide Unit
- Efficient instruction pipeline minimizes pipeline break latency
- Register and resource scoreboarding allow overlapped instruction execution
- 128-bit register bus speeds local register caching

- Two-way set associative, integrated instruction cache (80960JF is 4 Kbyte; 80960JA is 2 Kbyte)
- Direct-mapped, integrated data cache (80960JF is 2 Kbyte; 80960JA is 1 Kbyte)
- 1 Kbyte integrated data RAM delivers zero wait state program data

2.2 Burst Bus

A 32-bit high-performance bus controller interfaces the 80960JA/JF to external memory and peripherals. The Bus Control Unit fetches instructions and transfers data at the rate of up to four 32-bit words per six clock cycles. The external address/data bus is multiplexed.

Users may configure the 80960JA/JF's bus controller to match an application's fundamental memory organization. Physical bus width is register programmed for up to eight regions. Byte ordering and data caching are programmed through a group of logical memory templates and a defaults register.

The Bus Control Unit's features include:

- Multiplexed external bus to minimize pin count
- 32-, 16- and 8-bit bus widths to simplify I/O interfaces
- External ready control for address-to-data, data-to-data and data-to-next-address wait state types
- Support for big or little endian byte ordering to facilitate the porting of existing program code
- Unaligned bus accesses performed transparently
- Three-deep load/store queue to decouple the bus from the core

Upon reset, the 80960JA/JF conducts an internal self test. Then, before executing its first instruction, it performs an external bus confidence test by performing a checksum on the first words of the Initialization Boot Record.

The user may examine the contents of the caches at any time by executing special cache control instructions.

2.3 Timer Unit

The timer unit (TU) contains two independent 32-bit timers which are capable of counting at several clock rates and generating interrupts. Each is programmed by use of the Timer Unit registers. These memory-mapped registers are addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the 80960JA/JF's interrupt controller. The TU can generate a fault when unauthorized writes from user mode are detected. Clock prescaling is supported.

2.4 Priority Interrupt Controller

A programmable interrupt controller manages up to 240 external sources through an 8-bit external interrupt port. Alternatively, the interrupt inputs may be configured for individual edge- or level-triggered

inputs. The Interrupt Unit also accepts interrupts from the two on-chip timer channels and a single Non-Maskable Interrupt (NMI) pin. Interrupts are serviced according to their priority levels relative to the current process priority.

Low interrupt latency is critical to many embedded applications. As part of its highly flexible interrupt mechanism, the 80960JA/JF exploits several techniques to minimize latency:

- Interrupt vectors and interrupt handler routines can be reserved on-chip
- Register frames for high-priority interrupt handlers can be cached on-chip
- The interrupt stack can be placed in cacheable memory space

2.5 Instruction Set Summary

The 80960JA/JF adds several new instructions to the i960 core architecture. The new instructions are:

- Conditional Move
- Conditional Add
- Conditional Subtract
- Byte Swap
- Halt
- Cache Control
- Interrupt Control

Table 1 shows all instructions that are available.

2.6 Faults and Debugging

The 80960JA/JF employs a comprehensive fault model. The processor responds to faults by making implicit calls to a fault handling routine. Specific information collected for each fault allows the fault handler to diagnose exceptions and recover appropriately.

The processor also has built-in debug capabilities. In software, the 80960JA/JF may be configured to detect as many as seven different trace event types. Alternatively, **mark** and **fmark** instructions can generate trace events explicitly in the instruction stream. Hardware breakpoint registers are also available to trap on execution and data addresses.



2.7 Low Power Operation

Intel fabricates the 80960JA/JF using an advanced sub-micron manufacturing process. The processor's sub-micron topology provides the circuit density for optimal cache size and high operating speeds while dissipating modest power. The processor also uses dynamic power management to turn off clocks to unused circuits.

Users may program the 80960JA/JF to enter Halt mode for maximum power savings. In Halt mode, the processor core stops completely but the integrated peripherals continue to function, reducing overall power requirements up to 90 percent.

Processor execution resumes from internally or externally generated interrupts.

2.8 Test Features

The 80960JA/JF incorporates numerous features which enhance the user's ability to test both the processor and the system to which it is attached. These features include ONCE (On-Circuit Emulation) mode and Boundary Scan (JTAG).

The 80960JA/JF provides testability features compatible with IEEE Standard Test Access Port and Boundary Scan Architecture (IEEE Std. 1149.1).

One of the boundary scan instructions, HIGHZ, forces the processor to float all its output pins (ONCE mode). ONCE mode can also be initiated at reset without using the boundary scan mechanism.

ONCE mode is useful for board-level testing. This feature allows a mounted 80960JA/JF to electrically "remove" itself from a circuit board. This allows for system-level testing where a remote tester — such as an In-Circuit Emulator (ICE system) — can exercise the processor system.

The provided test logic does not interfere with component or circuit board behavior and ensures that components function correctly, connections between various components are correct, and various components interact correctly on the printed circuit board.

The JTAG Boundary Scan feature is an attractive alternative to conventional "bed-of-nails" testing. It can examine connections which might otherwise be inaccessible to a test system.

2.9 Memory-Mapped Control Registers

The 80960JA/JF, though compliant with i960 series processor core, has the added advantage of memory-mapped, internal control registers not found on the i960 Kx, Sx or Cx processors. These give software the interface to easily read and modify internal control registers.

Each of these registers is accessed as a memory-mapped, 32-bit register. Access is accomplished through regular memory-format instructions. The processor ensures that these accesses do not generate external bus cycles.

2.10 Data Types and Memory Addressing Modes

As with all i960 family processors, the 80960JA/JF instruction set supports several different data types and formats:

- Bit
- Bit fields
- Integer (8-, 16-, 32-, 64-bit)
- Ordinal (8-, 16-, 32-, 64-bit unsigned integers)
- Triple word (96 bits)
- Quad word (128 bits)

The 80960JA/JF provides a full set of addressing modes for C and assembly:

- Two Absolute modes
- Five Register Indirect modes
- Index with displacement
- IP with displacement

Table 1. 80960JA/JF Instruction Set

Data Movement	Arithmetic	Logical	Bit, Bit Field and Byte
Load Store Move *Conditional Select Load Address	Add Subtract Multiply Divide Remainder Modulo Shift Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry *Conditional Add *Conditional Subtract Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal *Byte Swap
Comparison	Branch	Call/Return	Fault
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	Processor Management	Atomic	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls *Halt System Control *Cache Control *Interrupt Control	Atomic Add Atomic Modify	

* Denotes new 80960Jx instructions unavailable on 80960CA/CF, 80960KA/KB and 80960SA/SB implementations.

3.0 PACKAGE INFORMATION

The 80960JA/JF will be offered in several speed and package grades. The following 132-pin Pin Grid Array (PGA) devices will be specified for operation at $V_{CC}=5.0V\pm 5\%$ over a case temperature range of 0° to 100°C:

- A80960JA/JF-33 (33.33 MHz)
- A80960JA/JF-25 (25 MHz)
- A80960JA/JF-16 (16 MHz)

The following 132-lead Plastic Quad Flatpack (PQFP) devices will be specified for operation at $V_{CC}=5.0V\pm 5\%$ over a case temperature range of 0° to 100°C:

- NG80960JA/JF-33 (33.33 MHz)
- NG80960JA/JF-25 (25 MHz)
- NG80960JA/JF-16 (16 MHz)

For complete package specifications and information, refer to Intel's *Packaging Handbook* (Order No. 240800).

3.1 Pin Descriptions

This section describes the pins for the 80960JA/JF in the 132-pin ceramic Pin Grid Array (PGA) package and 132-lead Plastic Quad Flatpack Package (PQFP).

Section 3.1.1, Functional Pin Definitions describes pin function; **Section 3.1.2, 80960JA/JF 132-Lead PGA Pinout** and **Section 3.1.3, 80960JA/JF PQFP Pinout** define the signal and pin locations for the supported package types.

3.1.1 Functional Pin Definitions

Table 2 presents the legend for interpreting the pin descriptions which follow. Pins associated with the bus interface are described in Table 3. Pins associated with basic control and test functions are described in Table 4. Pins associated with the Interrupt Unit are described in Table 5.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input pin only.
O	Output pin only.
I/O	Pin can be either an input or output.
–	Pin must be connected as described.
S	Synchronous. Inputs must meet setup and hold times relative to CLKIN for proper operation. S(E) Edge sensitive input S(L) Level sensitive input
A (...)	Asynchronous. Inputs may be asynchronous relative to CLKIN. A(E) Edge sensitive input A(L) Level sensitive input
R (...)	While the processor's RESET pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Q) is a valid output R(X) is driven to unknown state R(H) is pulled up to V_{CC}
H (...)	While the processor is in the hold state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Q) Maintains previous state or continues to be a valid output H(Z) Floats
P (...)	While the processor is halted, the pin: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Q) Maintains previous state or continues to be a valid output

Table 3. Pin Description — External Bus Signals (Sheet 1 of 3)

NAME	TYPE	DESCRIPTION															
AD31:0	I/O S(L) R(X) H(Z) P(Q)	<p>ADDRESS / DATA BUS carries 32-bit physical addresses and 8-, 16- or 32-bit data to and from memory. During an address (T_a) cycle, bits 2-31 contain a physical word address (bits 0-1 indicate SIZE; see below). During a data (T_d) cycle, read or write data is present on one or more contiguous bytes, comprising AD31:24, AD23:16, AD15:8 and AD7:0. During write operations, unused pins are driven to determinate values.</p> <p>SIZE, which comprises bits 0-1 of the AD lines during a T_a cycle, specifies the number of data transfers during the bus transaction.</p> <table border="1"> <thead> <tr> <th>AD1</th> <th>AD0</th> <th>Bus Transfers</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 Transfer</td> </tr> <tr> <td>0</td> <td>1</td> <td>2 Transfers</td> </tr> <tr> <td>1</td> <td>0</td> <td>3 Transfers</td> </tr> <tr> <td>1</td> <td>1</td> <td>4 Transfers</td> </tr> </tbody> </table> <p>When the processor enters Halt mode, if the previous bus operation was a:</p> <ul style="list-style-type: none"> • write — AD31:2 are driven with the last data value on the AD bus. • read — AD31:4 are driven with the last address value on the AD bus; AD3:2 are driven with the value of A3:2 from the last data cycle. <p>Typically, AD1:0 reflect the SIZE information of the last bus transaction (either instruction fetch or load/store) that was executed before entering Halt mode.</p>	AD1	AD0	Bus Transfers	0	0	1 Transfer	0	1	2 Transfers	1	0	3 Transfers	1	1	4 Transfers
AD1	AD0	Bus Transfers															
0	0	1 Transfer															
0	1	2 Transfers															
1	0	3 Transfers															
1	1	4 Transfers															
ALE	O R(0) H(Z) P(0)	ADDRESS LATCH ENABLE indicates the transfer of a physical address. ALE is asserted during a T_a cycle and deasserted before the beginning of the T_d state. It is active HIGH and floats to a high impedance state during a hold cycle (T_h).															
$\overline{\text{ALE}}$	O R(1) H(Z) P(1)	ADDRESS LATCH ENABLE indicates the transfer of a physical address. $\overline{\text{ALE}}$ is the inverted version of ALE. This signal gives the 80960JA/JF a high degree of compatibility with existing 80960Kx systems.															
$\overline{\text{ADS}}$	O R(1) H(Z) P(1)	ADDRESS STROBE indicates a valid address and the start of a new bus access. The processor asserts $\overline{\text{ADS}}$ for the entire T_a cycle. External bus control logic typically samples $\overline{\text{ADS}}$ at the end of the cycle.															
A3:2	O R(X) H(Z) P(Q)	<p>ADDRESS3:2 comprise a partial demultiplexed address bus.</p> <p><i>32-bit memory accesses:</i> the processor asserts address bits A3:2 during T_a. The partial word address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst.</p> <p><i>16-bit memory accesses:</i> the processor asserts address bits A3:1 during T_a with A1 driven on the $\overline{\text{BE1}}$ pin. The partial short word address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst.</p> <p><i>8-bit memory accesses:</i> the processor asserts address bits A3:0 during T_a, with A1:0 driven on $\overline{\text{BE1:0}}$. The partial byte address increments with each assertion of $\overline{\text{RDYRCV}}$ during a burst.</p>															

Table 3. Pin Description — External Bus Signals (Sheet 2 of 3)

NAME	TYPE	DESCRIPTION															
$\overline{\text{BE}}_{3:0}$	O R(1) H(Z) P(1)	<p>BYTE ENABLES select which of up to four data bytes on the bus participate in the current bus access. Byte enable encoding is dependent on the bus width of the memory region accessed:</p> <p><i>32-bit bus:</i></p> <ul style="list-style-type: none"> $\overline{\text{BE}}_3$ enables data on AD31:24 $\overline{\text{BE}}_2$ enables data on AD23:16 $\overline{\text{BE}}_1$ enables data on AD15:8 $\overline{\text{BE}}_0$ enables data on AD7:0 <p><i>16-bit bus:</i></p> <ul style="list-style-type: none"> $\overline{\text{BE}}_3$ becomes Byte High Enable (enables data on AD15:8) $\overline{\text{BE}}_2$ is not used (state is high) $\overline{\text{BE}}_1$ becomes Address Bit 1 (A1) $\overline{\text{BE}}_0$ becomes Byte Low Enable (enables data on AD7:0) <p><i>8-bit bus:</i></p> <ul style="list-style-type: none"> $\overline{\text{BE}}_3$ is not used (state is high) $\overline{\text{BE}}_2$ is not used (state is high) $\overline{\text{BE}}_1$ becomes Address Bit 1 (A1) $\overline{\text{BE}}_0$ becomes Address Bit 0 (A0) <p>The processor asserts byte enables, byte high enable and byte low enable during T_a. Since unaligned bus requests are split into separate bus transactions, these signals do not toggle during a burst. They remain active through the last T_d cycle.</p> <p>For accesses to 8- and 16-bit memory, the processor asserts the address bits in conjunction with A3:2 described above.</p>															
$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_{1:0}$	O R(X) H(Z) P(1)	<p>WIDTH/HALTED signals denote the physical memory attributes for a bus transaction:</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding-right: 20px;">$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_1$</td> <td style="padding-right: 20px;">$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_0$</td> <td></td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td>8 Bits Wide</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td>16 Bits Wide</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td>32 Bits Wide</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td>Processor Halted</td> </tr> </table> <p>The processor floats the $\overline{\text{WIDTH}}/\overline{\text{HLTD}}$ pins whenever it relinquishes the bus in response to a HOLD request, regardless of prior operating state.</p>	$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_1$	$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_0$		0	0	8 Bits Wide	0	1	16 Bits Wide	1	0	32 Bits Wide	1	1	Processor Halted
$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_1$	$\overline{\text{WIDTH}}/\overline{\text{HLTD}}_0$																
0	0	8 Bits Wide															
0	1	16 Bits Wide															
1	0	32 Bits Wide															
1	1	Processor Halted															
$\overline{\text{D/C}}$	O R(X) H(Z) P(Q)	<p>DATA/CODE indicates that a bus access is a data access (1) or an instruction access (0). $\overline{\text{D/C}}$ has the same timing as $\overline{\text{W/R}}$.</p>															
$\overline{\text{W/R}}$	O R(0) H(Z) P(Q)	<p>WRITE/READ specifies, during a T_a cycle, whether the operation is a write (1) or read (0). It is latched on-chip and remains valid during T_d cycles.</p>															
$\overline{\text{DT/R}}$	O R(0) H(Z) P(Q)	<p>DATA TRANSMIT / RECEIVE indicates the direction of data transfer to and from the address/data bus. It is low during T_a and T_w/T_d cycles for a read; it is high during T_a and T_w/T_d cycles for a write. $\overline{\text{DT/R}}$ never changes state when $\overline{\text{DEN}}$ is asserted.</p>															

Table 3. Pin Description — External Bus Signals (Sheet 3 of 3)

NAME	TYPE	DESCRIPTION
$\overline{\text{DEN}}$	O R(1) H(Z) P(1)	DATA ENABLE indicates data transfer cycles during a bus access. $\overline{\text{DEN}}$ is asserted at the start of the first data cycle in a bus access and deasserted at the end of the last data cycle. $\overline{\text{DEN}}$ is used with $\overline{\text{DT/R}}$ to provide control for data transceivers connected to the data bus.
$\overline{\text{BLAST}}$	O R(1) H(Z) P(1)	BURST LAST indicates the last transfer in a bus access. $\overline{\text{BLAST}}$ is asserted in the last data transfer of burst and non-burst accesses. $\overline{\text{BLAST}}$ remains active as long as wait states are inserted via the $\overline{\text{RDYRCV}}$ pin. $\overline{\text{BLAST}}$ becomes inactive after the final data transfer in a bus cycle.
$\overline{\text{RDYRCV}}$	I S(L)	READY/RECOVER indicates that data on AD lines can be sampled or removed. If $\overline{\text{RDYRCV}}$ is not asserted during a T_d cycle, the T_d cycle is extended to the next cycle by inserting a wait state (T_w). The $\overline{\text{RDYRCV}}$ pin has an alternate function during the recovery (T_r) state. The processor continues to insert additional recovery states until it samples the pin HIGH. This function allows slow external devices longer to float their buffers before the processor begins to drive address again.
$\overline{\text{LOCK/ONCE}}$	I/O S(L) R(H) H(Z) P(1)	BUS LOCK indicates that an atomic read-modify-write operation is in progress. The $\overline{\text{LOCK}}$ output is asserted in the first clock of an atomic operation and deasserted in the last data transfer of the sequence. The processor does not grant $\overline{\text{HOLDA}}$ while it is asserting $\overline{\text{LOCK}}$. This prevents external agents from accessing memory involved in semaphore operations. ONCE MODE: The processor samples the $\overline{\text{ONCE}}$ input during reset. If it is asserted LOW at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins. The pin has a weak internal pullup which is active during reset to ensure normal operation if the pin is left unconnected.
$\overline{\text{HOLD}}$	I S(L)	HOLD: A request from an external bus master to acquire the bus. When the processor receives $\overline{\text{HOLD}}$ and grants bus control to another master, it asserts $\overline{\text{HOLDA}}$, floats the address/data and control lines and enters the T_h state. When $\overline{\text{HOLD}}$ is deasserted, the processor deasserts $\overline{\text{HOLDA}}$ and enters either the T_i or T_a state, resuming control of the address/data and control lines.
$\overline{\text{HOLDA}}$	O R(Q) H(1) P(Q)	HOLD ACKNOWLEDGE indicates to an external bus master that the processor has relinquished control of the bus. The processor can grant $\overline{\text{HOLD}}$ requests and enter the T_h state during reset and while halted as well as during regular operation.
$\overline{\text{BSTAT}}$	O R(0) H(Q) P(0)	BUS STATUS indicates that the processor may soon stall unless it has sufficient access to the bus; see <i>i960[®] Jx Microprocessor User's Manual (272483)</i> . Arbitration logic can examine this signal to determine when an external bus master should acquire/relinquish the bus.

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 1 of 2)

NAME	TYPE	DESCRIPTION
CLKIN	I	CLOCK INPUT provides the processor's fundamental time base; both the processor core and the external bus run at the CLKIN rate. All input and output timings are specified relative to a rising CLKIN edge.
RESET	I A(L)	RESET initializes the processor and clears its internal logic. During reset, the processor places the address/data bus and control output pins in their idle (inactive) states. During reset, the input pins are ignored with the exception of $\overline{\text{LOCK/ONCE}}$, STEST and HOLD. The $\overline{\text{RESET}}$ pin has an internal synchronizer. To ensure predictable processor initialization during power up, $\overline{\text{RESET}}$ must be asserted a minimum of 10,000 CLKIN cycles with V_{CC} and CLKIN stable. On a warm reset, $\overline{\text{RESET}}$ should be asserted for a minimum of 15 cycles.
STEST	I S(L)	SELF TEST enables or disables the processor's internal self-test feature at initialization. STEST is examined at the end of reset. If STEST is asserted, the processor performs its internal self-test and the external bus confidence test. If STEST is deasserted, the processor performs only the external bus confidence test.
FAIL	O R(0) H(Q) P(1)	FAIL indicates a failure of the processor's built-in self-test performed during initialization. FAIL is asserted immediately upon reset and toggles during self-test to indicate the status of individual tests: <ul style="list-style-type: none"> • If self-test passes, the processor deasserts $\overline{\text{FAIL}}$ and commences operation from user code. • If self-test fails, the processor asserts $\overline{\text{FAIL}}$ and then stops executing.
TCK	I	TEST CLOCK is a CPU input which provides the clocking function for IEEE 1149.1 Boundary Scan Testing (JTAG). State information and data are clocked into the processor on the rising edge; data is clocked out of the processor on the falling edge.
TDI	I S(L)	TEST DATA INPUT is the serial input pin for JTAG. TDI is sampled on the rising edge of TCK, during the SHIFT-IR and SHIFT-DR states of the Test Access Port.
TDO	O R(Q) H(Q) P(Q)	TEST DATA OUTPUT is the serial output pin for JTAG. TDO is driven on the falling edge of TCK during the SHIFT-IR and SHIFT-DR states of the Test Access Port. At other times, TDO floats. TDO does not float during ONCE mode.
TRST	I A(L)	TEST RESET asynchronously resets the Test Access Port (TAP) controller function of IEEE 1149.1 Boundary Scan testing (JTAG). If using the Boundary Scan feature, connect a pulldown resistor between this pin and ground. If the Test Access Port will not be used, the pin can be tied directly to ground.

Table 4. Pin Description — Processor Control Signals, Test Signals and Power (Sheet 2 of 2)

NAME	TYPE	DESCRIPTION
TMS	I S(L)	TEST MODE SELECT is sampled at the rising edge of TCK to select the operation of the test logic for IEEE 1149.1 Boundary Scan testing.
V _{CC}	–	POWER leads intended for external connection to a V _{CC} board plane.
V _{CCPLL}	–	PLL POWER is a separate V _{CC} supply lead for the phase lock loop clock generator. It is intended for external connection to the V _{CC} board plane. In noisy environments, add a simple bypass filter circuit to reduce noise-induced clock jitter and its effects on timing relationships.
V _{SS}	–	GROUND leads intended for external connection to a V _{SS} board plane.
N.C.	–	NO CONNECT leads. Do not make any system connections to these leads.

Table 5. Pin Description — Interrupt Unit Signals

NAME	TYPE	DESCRIPTION
$\overline{\text{XINT7:0}}$	I A(E/L)	<p>EXTERNAL INTERRUPT pins are used to request interrupt service. The $\overline{\text{XINT7:0}}$ pins can be configured in three modes:</p> <p>Dedicated Mode: Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low or high) or edge (rising or falling) sensitive.</p> <p>Expanded Mode: All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode.</p> <p>Mixed Mode: The $\overline{\text{XINT7:5}}$ pins act as dedicated sources and the $\overline{\text{XINT4:0}}$ pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to 010₂ internally.</p> <p>Unused external interrupt pins should be connected to V_{CC}.</p>
$\overline{\text{NMI}}$	I A(E)	<p>NON-MASKABLE INTERRUPT causes a non-maskable interrupt event to occur. NMI is the highest priority interrupt source and is falling edge-triggered. If NMI is unused, it should be connected to V_{CC}.</p>

3.1.2 80960JA/JF 132-Lead PGA Pinout

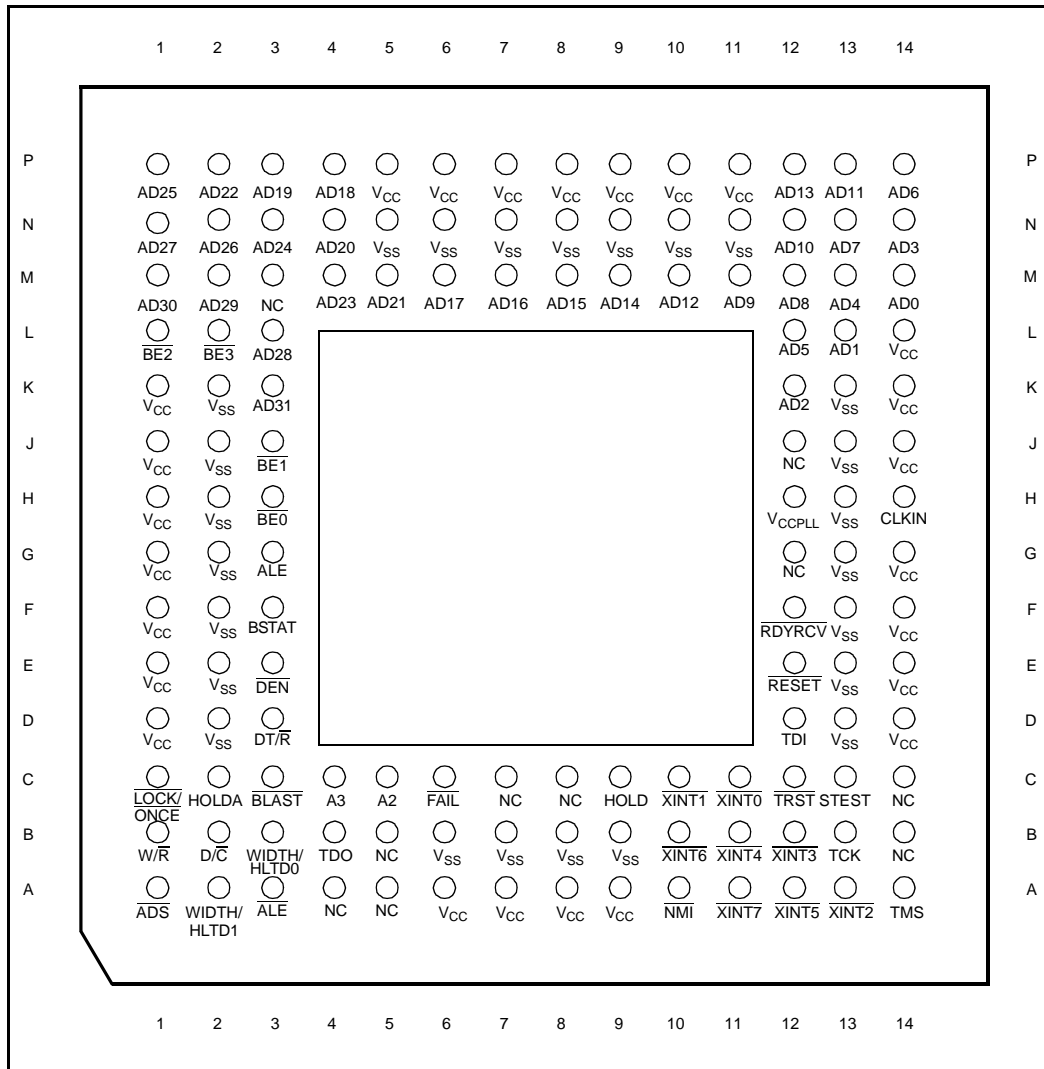


Figure 3. 132-Lead Pin Grid Array Bottom View - Pins Facing Up

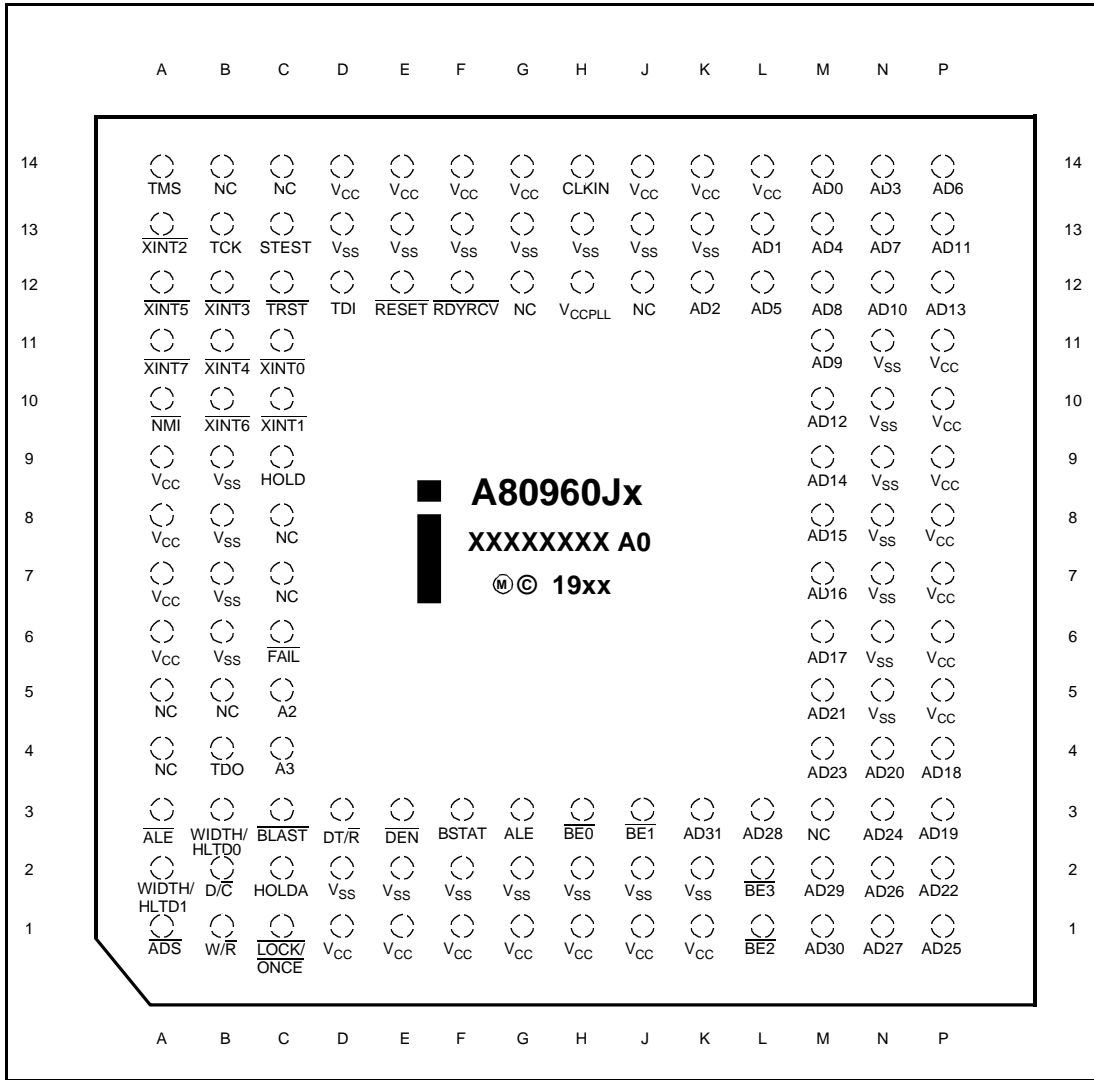


Figure 4. 132-Lead Pin Grid Array Top View - Pins Facing Down

Table 6. 132-Lead PGA Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
A2	C5	AD31	K3	TDI	D12	V _{SS}	B9
A3	C4	$\overline{\text{ADS}}$	A1	TDO	B4	V _{SS}	D2
AD0	M14	ALE	G3	TMS	A14	V _{SS}	D13
AD1	L13	$\overline{\text{ALE}}$	A3	$\overline{\text{TRST}}$	C12	V _{SS}	E2
AD2	K12	$\overline{\text{BE0}}$	H3	V _{CC}	A6	V _{SS}	E13
AD3	N14	$\overline{\text{BE1}}$	J3	V _{CC}	A7	V _{SS}	F2
AD4	M13	$\overline{\text{BE2}}$	L1	V _{CC}	A8	V _{SS}	F13
AD5	L12	$\overline{\text{BE3}}$	L2	V _{CC}	A9	V _{SS}	G2
AD6	P14	$\overline{\text{BLAST}}$	C3	V _{CC}	D1	V _{SS}	G13
AD7	N13	BSTAT	F3	V _{CC}	D14	V _{SS}	H2
AD8	M12	CLKIN	H14	V _{CC}	E1	V _{SS}	H13
AD9	M11	$\overline{\text{D/C}}$	B2	V _{CC}	E14	V _{SS}	J2
AD10	N12	$\overline{\text{DEN}}$	E3	V _{CC}	F1	V _{SS}	J13
AD11	P13	$\overline{\text{DT/R}}$	D3	V _{CC}	F14	V _{SS}	K2
AD12	M10	$\overline{\text{FAIL}}$	C6	V _{CC}	G1	V _{SS}	K13
AD13	P12	HOLD	C9	V _{CC}	G14	V _{SS}	N5
AD14	M9	HOLDA	C2	V _{CC}	H1	V _{SS}	N6
AD15	M8	$\overline{\text{LOCK/ONCE}}$	C1	V _{CC}	J1	V _{SS}	N7
AD16	M7	NC	A4	V _{CC}	J14	V _{SS}	N8
AD17	M6	NC	A5	V _{CC}	K1	V _{SS}	N9
AD18	P4	NC	B5	V _{CC}	K14	V _{SS}	N10
AD19	P3	NC	B14	V _{CC}	L14	V _{SS}	N11
AD20	N4	NC	C7	V _{CC}	P5	$\overline{\text{W/R}}$	B1
AD21	M5	NC	C8	V _{CC}	P6	WIDTH/HLTD0	B3
AD22	P2	NC	C14	V _{CC}	P7	WIDTH/HLTD1	A2
AD23	M4	NC	G12	V _{CC}	P8	$\overline{\text{XINT0}}$	C11
AD24	N3	NC	J12	V _{CC}	P9	$\overline{\text{XINT1}}$	C10
AD25	P1	NC	M3	V _{CC}	P10	$\overline{\text{XINT2}}$	A13
AD26	N2	$\overline{\text{NM}}$	A10	V _{CC}	P11	$\overline{\text{XINT3}}$	B12
AD27	N1	$\overline{\text{RDYRCV}}$	F12	V _{CCPLL}	H12	$\overline{\text{XINT4}}$	B11
AD28	L3	$\overline{\text{RESET}}$	E12	V _{SS}	B6	$\overline{\text{XINT5}}$	A12
AD29	M2	STEST	C13	V _{SS}	B7	$\overline{\text{XINT6}}$	B10
AD30	M1	TCK	B13	V _{SS}	B8	$\overline{\text{XINT7}}$	A11

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 7. 132-Lead PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	$\overline{\text{ADS}}$	C6	$\overline{\text{FAIL}}$	H1	V_{CC}	M10	AD12
A2	WIDTH/HLTD1	C7	NC	H2	V_{SS}	M11	AD9
A3	$\overline{\text{ALE}}$	C8	NC	H3	$\overline{\text{BE0}}$	M12	AD8
A4	NC	C9	HOLD	H12	V_{CCPLL}	M13	AD4
A5	NC	C10	$\overline{\text{XINT1}}$	H13	V_{SS}	M14	AD0
A6	V_{CC}	C11	$\overline{\text{XINT0}}$	H14	CLKIN	N1	AD27
A7	V_{CC}	C12	$\overline{\text{TRST}}$	J1	V_{CC}	N2	AD26
A8	V_{CC}	C13	STEST	J2	V_{SS}	N3	AD24
A9	V_{CC}	C14	NC	J3	$\overline{\text{BE1}}$	N4	AD20
A10	$\overline{\text{NMI}}$	D1	V_{CC}	J12	NC	N5	V_{SS}
A11	$\overline{\text{XINT7}}$	D2	V_{SS}	J13	V_{SS}	N6	V_{SS}
A12	$\overline{\text{XINT5}}$	D3	DT/ $\overline{\text{R}}$	J14	V_{CC}	N7	V_{SS}
A13	$\overline{\text{XINT2}}$	D12	TDI	K1	V_{CC}	N8	V_{SS}
A14	TMS	D13	V_{SS}	K2	V_{SS}	N9	V_{SS}
B1	$\overline{\text{W/R}}$	D14	V_{CC}	K3	AD31	N10	V_{SS}
B2	D/ $\overline{\text{C}}$	E1	V_{CC}	K12	AD2	N11	V_{SS}
B3	WIDTH/HLTD0	E2	V_{SS}	K13	V_{SS}	N12	AD10
B4	TDO	E3	$\overline{\text{DEN}}$	K14	V_{CC}	N13	AD7
B5	NC	E12	$\overline{\text{RESET}}$	L1	$\overline{\text{BE2}}$	N14	AD3
B6	V_{SS}	E13	V_{SS}	L2	$\overline{\text{BE3}}$	P1	AD25
B7	V_{SS}	E14	V_{CC}	L3	AD28	P2	AD22
B8	V_{SS}	F1	V_{CC}	L12	AD5	P3	AD19
B9	V_{SS}	F2	V_{SS}	L13	AD1	P4	AD18
B10	$\overline{\text{XINT6}}$	F3	BSTAT	L14	V_{CC}	P5	V_{CC}
B11	$\overline{\text{XINT4}}$	F12	$\overline{\text{RDYRCV}}$	M1	AD30	P6	V_{CC}
B12	$\overline{\text{XINT3}}$	F13	V_{SS}	M2	AD29	P7	V_{CC}
B13	TCK	F14	V_{CC}	M3	NC	P8	V_{CC}
B14	NC	G1	V_{CC}	M4	AD23	P9	V_{CC}
C1	$\overline{\text{LOCK/ONCE}}$	G2	V_{SS}	M5	AD21	P10	V_{CC}
C2	HOLDA	G3	ALE	M6	AD17	P11	V_{CC}
C3	$\overline{\text{BLAST}}$	G12	NC	M7	AD16	P12	AD13
C4	A3	G13	V_{SS}	M8	AD15	P13	AD11
C5	A2	G14	V_{CC}	M9	AD14	P14	AD6

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.1.3 80960JA/JF PQFP Pinout

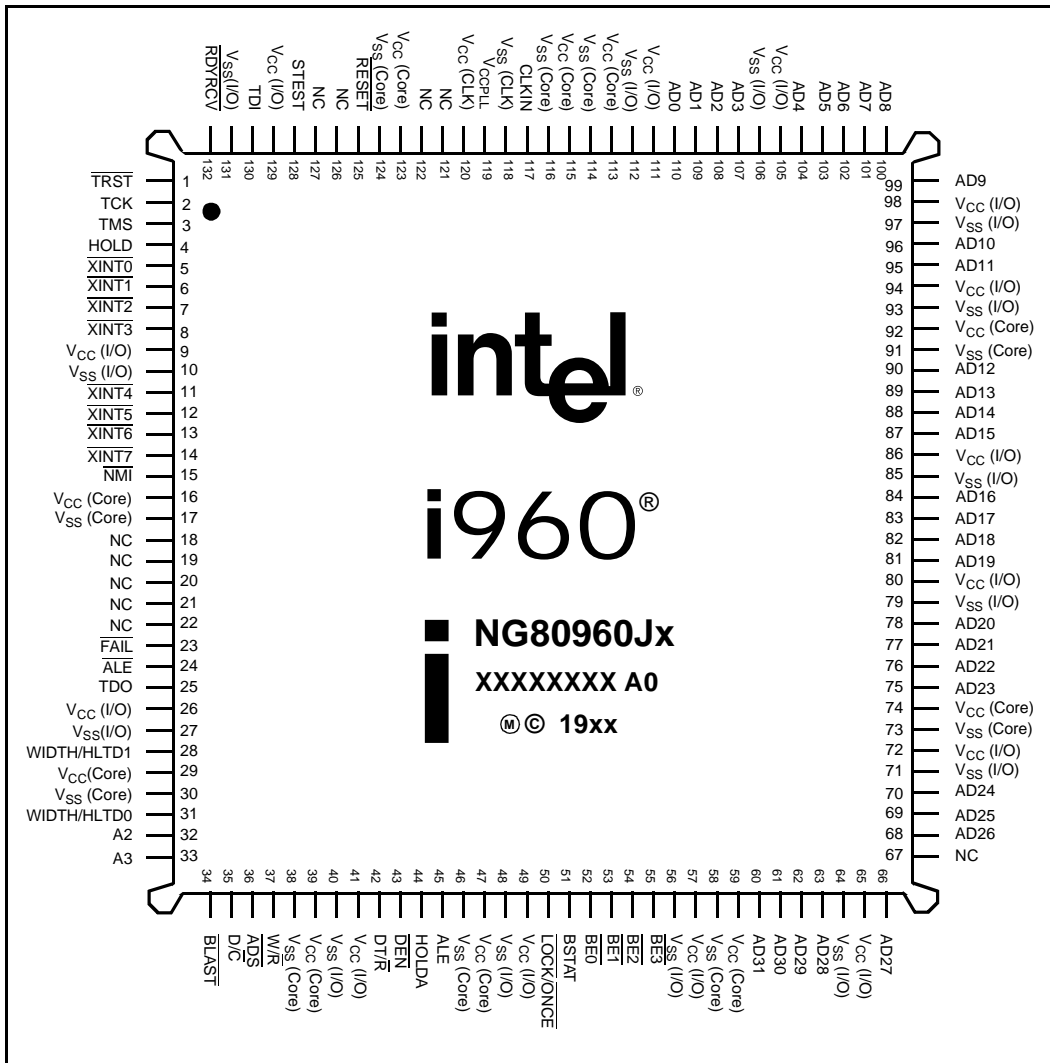


Figure 5. 132-Lead PQFP - Top View

Table 8. 132-Lead PQFP Pinout — In Signal Order

Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin
AD31	60	$\overline{\text{ALE}}$	24	V_{CC} (Core)	47	V_{SS} (I/O)	10
AD30	61	$\overline{\text{ADS}}$	36	V_{CC} (Core)	59	V_{SS} (I/O)	27
AD29	62	A3	33	V_{CC} (Core)	74	V_{SS} (I/O)	40
AD28	63	A2	32	V_{CC} (Core)	92	V_{SS} (I/O)	48
AD27	66	$\overline{\text{BE3}}$	55	V_{CC} (Core)	113	V_{SS} (I/O)	56
AD26	68	$\overline{\text{BE2}}$	54	V_{CC} (Core)	115	V_{SS} (I/O)	64
AD25	69	$\overline{\text{BE1}}$	53	V_{CC} (Core)	123	V_{SS} (I/O)	71
AD24	70	$\overline{\text{BE0}}$	52	V_{CC} (I/O)	9	V_{SS} (I/O)	79
AD23	75	WIDTH/HLTD1	28	V_{CC} (I/O)	26	V_{SS} (I/O)	85
AD22	76	WIDTH/HLTD0	31	V_{CC} (I/O)	41	V_{SS} (I/O)	93
AD21	77	$\overline{\text{D/C}}$	35	V_{CC} (I/O)	49	V_{SS} (I/O)	97
AD20	78	$\overline{\text{W/R}}$	37	V_{CC} (I/O)	57	V_{SS} (I/O)	106
AD19	81	$\overline{\text{DT/R}}$	42	V_{CC} (I/O)	65	V_{SS} (I/O)	112
AD18	82	$\overline{\text{DEN}}$	43	V_{CC} (I/O)	72	V_{SS} (I/O)	131
AD17	83	$\overline{\text{BLAST}}$	34	V_{CC} (I/O)	80	NC	18
AD16	84	$\overline{\text{RDYRCV}}$	132	V_{CC} (I/O)	86	NC	19
AD15	87	$\overline{\text{LOCK/ONCE}}$	50	V_{CC} (I/O)	94	NC	20
AD14	88	HOLD	4	V_{CC} (I/O)	98	NC	21
AD13	89	HOLDA	44	V_{CC} (I/O)	105	NC	22
AD12	90	BSTAT	51	V_{CC} (I/O)	111	NC	67
AD11	95	CLKIN	117	V_{CC} (I/O)	129	NC	121
AD10	96	$\overline{\text{RESET}}$	125	V_{CCPLL}	119	NC	122
AD9	99	STEST	128	V_{SS} (CLK)	118	NC	126
AD8	100	FAIL	23	V_{SS} (Core)	17	NC	127
AD7	101	TCK	2	V_{SS} (Core)	30	$\overline{\text{XINT7}}$	14
AD6	102	TDI	130	V_{SS} (Core)	38	$\overline{\text{XINT6}}$	13
AD5	103	TDO	25	V_{SS} (Core)	46	$\overline{\text{XINT5}}$	12
AD4	104	$\overline{\text{TRST}}$	1	V_{SS} (Core)	58	$\overline{\text{XINT4}}$	11
AD3	107	TMS	3	V_{SS} (Core)	73	$\overline{\text{XINT3}}$	8
AD2	108	V_{CC} (CLK)	120	V_{SS} (Core)	91	$\overline{\text{XINT2}}$	7
AD1	109	V_{CC} (Core)	16	V_{SS} (Core)	114	$\overline{\text{XINT1}}$	6
AD0	110	V_{CC} (Core)	29	V_{SS} (Core)	116	$\overline{\text{XINT0}}$	5
ALE	45	V_{CC} (Core)	39	V_{SS} (Core)	124	$\overline{\text{NMI}}$	15

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

Table 9. 132-Lead PQFP Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	$\overline{\text{TRST}}$	34	$\overline{\text{BLAST}}$	67	NC	100	AD8
2	TCK	35	$\overline{\text{D/C}}$	68	AD26	101	AD7
3	TMS	36	$\overline{\text{ADS}}$	69	AD25	102	AD6
4	HOLD	37	$\overline{\text{W/R}}$	70	AD24	103	AD5
5	$\overline{\text{XINT0}}$	38	V_{SS} (Core)	71	V_{SS} (I/O)	104	AD4
6	$\overline{\text{XINT1}}$	39	V_{CC} (Core)	72	V_{CC} (I/O)	105	V_{CC} (I/O)
7	$\overline{\text{XINT2}}$	40	V_{SS} (I/O)	73	V_{SS} (Core)	106	V_{SS} (I/O)
8	$\overline{\text{XINT3}}$	41	V_{CC} (I/O)	74	V_{CC} (Core)	107	AD3
9	V_{CC} (I/O)	42	$\overline{\text{DT/R}}$	75	AD23	108	AD2
10	V_{SS} (I/O)	43	$\overline{\text{DEN}}$	76	AD22	109	AD1
11	$\overline{\text{XINT4}}$	44	HOLDA	77	AD21	110	AD0
12	$\overline{\text{XINT5}}$	45	ALE	78	AD20	111	V_{CC} (I/O)
13	$\overline{\text{XINT6}}$	46	V_{SS} (Core)	79	V_{SS} (I/O)	112	V_{SS} (I/O)
14	$\overline{\text{XINT7}}$	47	V_{CC} (Core)	80	V_{CC} (I/O)	113	V_{CC} (Core)
15	$\overline{\text{NMI}}$	48	V_{SS} (I/O)	81	AD19	114	V_{SS} (Core)
16	V_{CC} (Core)	49	V_{CC} (I/O)	82	AD18	115	V_{CC} (Core)
17	V_{SS} (Core)	50	$\overline{\text{LOCK/ONCE}}$	83	AD17	116	V_{SS} (Core)
18	NC	51	BSTAT	84	AD16	117	CLKIN
19	NC	52	$\overline{\text{BE0}}$	85	V_{SS} (I/O)	118	V_{SS} (CLK)
20	NC	53	$\overline{\text{BE1}}$	86	V_{CC} (I/O)	119	V_{CC} PLL
21	NC	54	$\overline{\text{BE2}}$	87	AD15	120	V_{CC} (CLK)
22	NC	55	$\overline{\text{BE3}}$	88	AD14	121	NC
23	$\overline{\text{FAIL}}$	56	V_{SS} (I/O)	89	AD13	122	NC
24	$\overline{\text{ALE}}$	57	V_{CC} (I/O)	90	AD12	123	V_{CC} (Core)
25	TDO	58	V_{SS} (Core)	91	V_{SS} (Core)	124	V_{SS} (Core)
26	V_{CC} (I/O)	59	V_{CC} (Core)	92	V_{CC} (Core)	125	$\overline{\text{RESET}}$
27	V_{SS} (I/O)	60	AD31	93	V_{SS} (I/O)	126	NC
28	WIDTH/HLTD1	61	AD30	94	V_{CC} (I/O)	127	NC
29	V_{CC} (Core)	62	AD29	95	AD11	128	STEST
30	V_{SS} (Core)	63	AD28	96	AD10	129	V_{CC} (I/O)
31	WIDTH/HLTD0	64	V_{SS} (I/O)	97	V_{SS} (I/O)	130	TDI
32	A2	65	V_{CC} (I/O)	98	V_{CC} (I/O)	131	V_{SS} (I/O)
33	A3	66	AD27	99	AD9	132	$\overline{\text{RDYRCV}}$

NOTE: Do not connect any external logic to pins marked NC (no connect pins).

3.2 Package Thermal Specifications

The 80960JA/JF is specified for operation when T_C (case temperature) is within the range of 0°C to 100°C. Case temperature may be measured in any environment to determine whether the 80960JA/JF is within specified operating range. The case temperature should be measured at the center of the top surface, opposite the pins.

θ_{CA} is the thermal resistance from case to ambient. Use the following equation to calculate T_A , the maximum ambient temperature to conform to a particular case temperature:

$$T_A = T_C - P (\theta_{CA})$$

Junction temperature, T_J , is commonly used in reliability calculations. T_J can be calculated from θ_{JC} (thermal resistance from junction to case) using the following equation:

$$T_J = T_C + P (\theta_{JC})$$

Similarly, if T_A is known, the corresponding case temperature, T_C , can be calculated as follows:

$$T_C = T_A + P (\theta_{CA})$$

Compute P by multiplying I_{CC} (the typical current) from Table 13 and a V_{CC} of 5 V. Values for θ_{JC} and θ_{CA} are given in Table 10 for the PGA package and Table 11 for the PQFP package. Note that the processor's θ_{JA} for the ceramic PGA package may be significantly reduced by adding a heatsink.

Table 10. 132-Lead PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.08)
θ_{JC} (Junction-to-Case)	3	3	3	3	3	3
θ_{CA} (Case-to-Ambient) (No Heatsink)	18	15	12	11	11	11
θ_{CA} (Case-to-Ambient) (Omnidirectional Heatsink)	15	12	9	8	8	8
θ_{CA} (Case-to-Ambient) (Unidirectional Heatsink)	14	11	8	7	7	7

NOTES:

1. This table applies to a PGA device plugged into a socket or soldered directly into a board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{J-CAP} = 4^\circ\text{C/W}$ (approx.)
4. $\theta_{J-PIN} = 4^\circ\text{C/W}$ (inner pins) (approx.)
5. $\theta_{J-PIN} = 8^\circ\text{C/W}$ (outer pins) (approx.)

Table 11. 132-Lead PQFP Package Thermal Characteristics

Thermal Resistance — °C/Watt							
Parameter	Airflow — ft./min (m/sec)						
	0 (0)	50 (0.25)	100 (0.50)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
θ_{JC} (Junction-to-Case)	6	7	7	7	7	7	7
θ_{CA} (Case-to-Ambient -No Heatsink)	23	20	18	14	10	9	8

NOTES:

1. This table applies to a PQFP device soldered directly into board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$
3. $\theta_{JL} = 18^{\circ}\text{C/W}$ (approx.)
4. $\theta_{JB} = 18^{\circ}\text{C/W}$ (approx.)

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	-65°C to +150°C
Case Temperature Under Bias	-65°C to +110°C
Supply Voltage wrt. V _{SS}	-0.5V to + 6.5V
Voltage on Other Pins wrt. V _{SS}	-0.5V to V _{CC} + 0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Contact your local Intel representative before finalizing a design.

WARNING: *Stressing the device beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only. Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.*

4.2 Operating Conditions

Table 12. Targeted 80960JA/JF Operating Conditions

Symbol	Parameter	Min	Max	Units	Notes
V _{CC}	Supply Voltage			V	
	80960JA/JF-33	4.75	5.25		
	80960JA/JF-25	4.75	5.25		
	80960JA/JF-16	4.75	5.25		
f _{CLKIN}	Input Clock Frequency			MHz	
	80960JA/JF-33	8	33.33		
	80960JA/JF-25	8	25		
	80960JA/JF-16	8	16.67		
T _C	Operating Case Temperature			°C	
	A80960JA/JF-33 (132 PGA)	0	100		
	NG80960JA/JF-33 (132 PQFP)	0	100		
	A80960JA/JF-25 (132 PGA)	0	100		
	NG80960JA/JF-25 (132 PQFP)	0	100		
	A80960JA/JF-16 (132 PGA)	0	100		
NG80960JA/JF-16 (132 PQFP)	0	100			

4.3 Connection Recommendations

For clean on-chip power distribution, V_{CC} and V_{SS} pins separately feed the device's functional units. Power and ground connections must be made to all 80960JA/JF power and ground pins. On the circuit board, every V_{CC} pin should connect to a power plane and every V_{SS} pin should connect to a ground plane. Place liberal decoupling capacitance near the 80960JA/JF, since the processor can cause transient power surges.

Pay special attention to the Test Reset ($\overline{\text{TRST}}$) pin. It is necessary to reset the Test Access Port (TAP) controller even if it will not be used. The easiest method is connecting a pull-down resistor between the $\overline{\text{TRST}}$ pin and ground. If the JTAG Boundary Scan function will not be used (even for board-level testing), it is permissible to connect $\overline{\text{TRST}}$ directly to ground.

Pins identified as NC must not be connected in the system.

ADVANCE INFORMATION

4.4 DC Specifications

Table 13. Targeted 80960JA/JF DC Characteristics (Sheet 1 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		$V_{CC} + 0.3$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 5 \text{ mA}$
V_{OH}	Output High Voltage	2.4 $V_{CC} - 0.5$			V	$I_{OH} = -1 \text{ mA}$ $I_{OH} = -200 \mu\text{A}$
I_{LI1}	Input Leakage Current for each pin except TCK, TDI, $\overline{\text{TRST}}$ and TMS			± 5	μA	$0 \leq V_{IN} \leq V_{CC}$
I_{LI2}	Input Leakage Current for TCK, TDI, $\overline{\text{TRST}}$ and TMS		-140	-250	μA	$V_{IN} = 0.45\text{V}$ (1)
I_{LO}	Output Leakage Current			± 5	μA	$0.4 \leq V_{OUT} \leq V_{CC}$
I_{CC}	Power Supply Current (80960JA/JF-33) I_{CC} Operating I_{CC} Halt mode I_{CC} ONCE mode	325	420 36 19	515 40 30	mA	(2,3,4,5) (4,5) (4,5)
I_{CC}	Power Supply Current (80960JA/JF-25) I_{CC} Operating I_{CC} Halt mode I_{CC} ONCE mode	250	325 27 19	390 30 30	mA	(2,3,4,5) (4,5) (4,5)
I_{CC}	Power Supply Current (80960JA/JF-16) I_{CC} Operating I_{CC} Halt Mode I_{CC} ONCE Mode	170	205 18 19	245 20 30	mA	(2,3,4,5) (4,5) (4,5)

NOTES:

1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 6, AC Test Load (pg. 25).
3. I_{CC} Minimum is measured at minimum V_{CC} and maximum temperature. This parameter is characterized but not tested.
4. I_{CC} Typical is measured at nominal V_{CC} and $T_C = 25 \text{ }^\circ\text{C}$. This parameter is characterized but not tested.
5. I_{CC} Maximum is measured at maximum V_{CC} and minimum temperature. This parameter is fully tested.
6. Not tested.

Table 13. Targeted 80960JA/JF DC Characteristics (Sheet 2 of 2)

Symbol	Parameter	Min	Typ	Max	Units	Notes
C _{IN}	Input Capacitance			12	pF	f _{CLKIN} = f _{MIN} (6)
	PGA PQFP			10		
C _{OUT}	I/O or Output Capacitance			12	pF	f _{CLKIN} = f _{MIN} (6)
	PGA PQFP			10		
C _{CLK}	CLKIN Capacitance			12	pF	f _{CLKIN} = f _{MIN} (6)
	PGA PQFP			10		

NOTES:

1. These pins have internal pullup devices. Typical leakage current is not tested.
2. Measured with device operating and outputs loaded to the test condition in Figure 6, AC Test Load (pg. 25).
3. I_{CC} Minimum is measured at minimum V_{CC} and maximum temperature. This parameter is characterized but not tested.
4. I_{CC} Typical is measured at nominal V_{CC} and T_C = 25 °C. This parameter is characterized but not tested.
5. I_{CC} Maximum is measured at maximum V_{CC} and minimum temperature. This parameter is fully tested.
6. Not tested.

4.5 AC Specifications

Targeted 80960JA/JF AC timings are based upon design simulation at 33 MHz. Revised information for all frequency grades will be published upon the completion of device characterization. Contact your local Intel representative before finalizing a design.

Table 14. Targeted 80960JA/JF Input Clock Timings

Symbol	Parameter	Min	Max	Units	Notes
T _F	CLKIN Frequency	8	33.33	MHz	
T _C	CLKIN Period	30	62.5	ns	
T _{CS}	CLKIN Period Stability		±0.1	%Δ	Adjacent Clocks (1)
T _{CH}	CLKIN High Time	12		ns	Measured at 1.5 V (1)
T _{CL}	CLKIN Low Time	12		ns	Measured at 1.5 V (1)
T _{CR}	CLKIN Rise Time		4	ns	0.8 V to 2.0 V (1)
T _{CF}	CLKIN Fall Time		4	ns	2.0 V to 0.8 V (1)

NOTES:

1. Not tested.

Table 15. Targeted 80960JA/JF Synchronous Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{OV1}	Output Valid Delay, Except ALE/ $\overline{\text{ALE}}$ Inactive and DT/ $\overline{\text{R}}$	3	15	ns	
T _{OV2}	Output Valid Delay, DT/ $\overline{\text{R}}$	0.5 T _C + 3	0.5 T _C + 15	ns	
T _{OF}	Output Float Delay	3	13	ns	(1)

NOTES:

1. A float condition occurs when the output current becomes less than I_{LO}. Float delay is not tested.

Table 16. Targeted 80960JA/JF Synchronous Input Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{IS1}	Input Setup to CLKIN — AD31:0, $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$	6		ns	(1)
T _{IH1}	Input Hold from CLKIN — AD31:0, $\overline{\text{NMI}}$, $\overline{\text{XINT7:0}}$	2		ns	(1)
T _{IS2}	Input Setup to CLKIN — $\overline{\text{RDYRCV}}$ and HOLD	8		ns	(2)
T _{IH2}	Input Hold from CLKIN — $\overline{\text{RDYRCV}}$ and HOLD	1		ns	(2)
T _{IS3}	Input Setup to CLKIN — $\overline{\text{RESET}}$	6		ns	(3)
T _{IH3}	Input Hold from CLKIN — $\overline{\text{RESET}}$	2		ns	(3)
T _{IS4}	Input Setup to $\overline{\text{RESET}}$ — $\overline{\text{ONCE}}$, STEST	6		ns	(4)
T _{IH4}	Input Hold from $\overline{\text{RESET}}$ — $\overline{\text{ONCE}}$, STEST	2		ns	(4)

NOTES:

1. AD31:0 are synchronous inputs. Setup and hold times must be met for proper processor operation. $\overline{\text{NMI}}$ and $\overline{\text{XINT7:0}}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge. For asynchronous operation, $\overline{\text{NMI}}$ and $\overline{\text{XINT7:0}}$ must be asserted for a minimum of two CLKIN periods to guarantee recognition.
2. $\overline{\text{RDYRCV}}$ and HOLD are synchronous inputs. Setup and hold times must be met for proper processor operation.
3. $\overline{\text{RESET}}$ may be synchronous or asynchronous. Meeting setup and hold time guarantees recognition at a particular clock edge.
4. $\overline{\text{ONCE}}$ and STEST must be stable at the rising edge of $\overline{\text{RESET}}$ for proper operation.

Table 17. Targeted 80960JA/JF Relative Output Timings

Symbol	Parameter	Min	Max	Units	Notes
T _{LXL}	ALE/ $\overline{\text{ALE}}$ Width	0.5 T _C - 3		ns	(1)
T _{LXA}	Address Hold from ALE/ $\overline{\text{ALE}}$ Inactive	0.5 T _C - 3		ns	Equal Loading (1)
T _{DXD}	DT/ $\overline{\text{R}}$ Valid to $\overline{\text{DEN}}$ Active	0.5 T _C - 3		ns	Equal Loading (1)

NOTES:

1. Guaranteed by design. May not be 100% tested.

Table 18. Targeted 80960JA/JF Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency		8	MHz	
T_{BSC}	TCK Period	125		ns	
T_{BSCH}	TCK High Time	40		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	40		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		8	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		8	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	8		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	10		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	Relative to falling edge of TCK
T_{BSOF1}	TDO Float Delay	3	36	ns	Relative to falling edge of TCK
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to falling edge of TCK
T_{BSOF2}	All Outputs (Non-Test) Float Delay	3	36	ns	Relative to falling edge of TCK
T_{BSIS2}	Input Setup to TCK — All Inputs (Non-Test)	8		ns	
T_{BSIH2}	Input Hold from TCK — All Inputs (Non-Test)	10		ns	

NOTES:

1. Not tested.

4.5.1 AC Test Conditions and Derating Curves

The AC Specifications in **Section 4.5, AC Specifications** are tested with the 50 pF load indicated in Figure 6. Figure 7 shows how timings vary with load capacitance; Figure 8 shows how output rise and fall times vary with load capacitance.

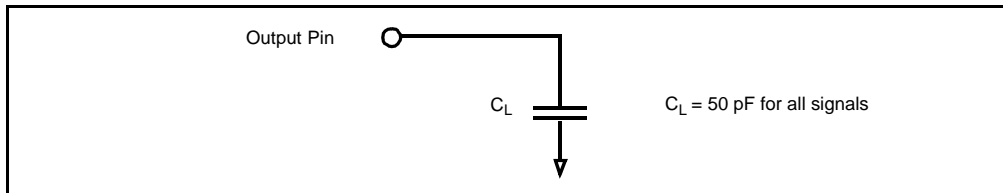


Figure 6. AC Test Load

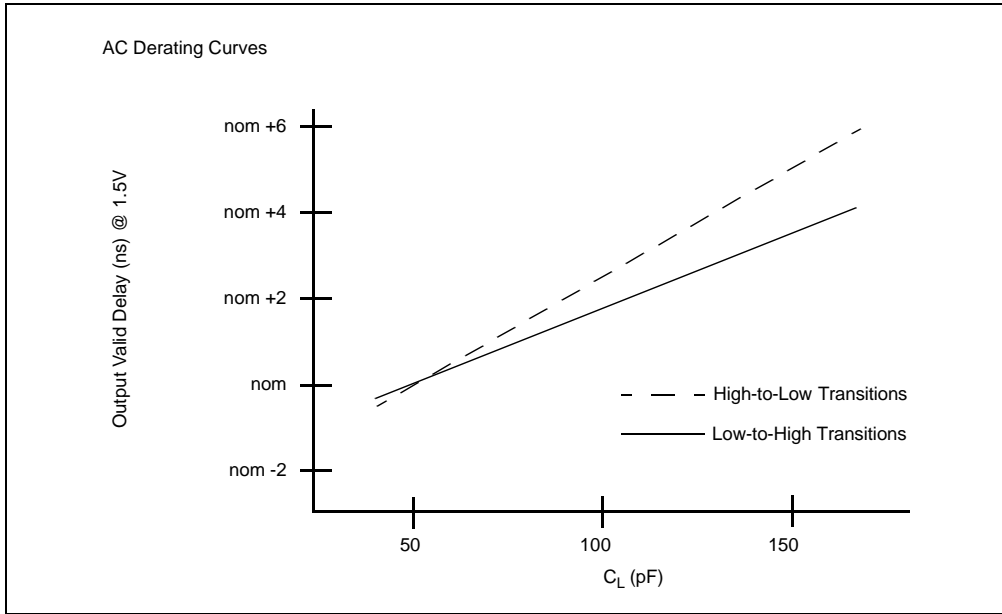


Figure 7. Output Delay or Hold vs. Load Capacitance

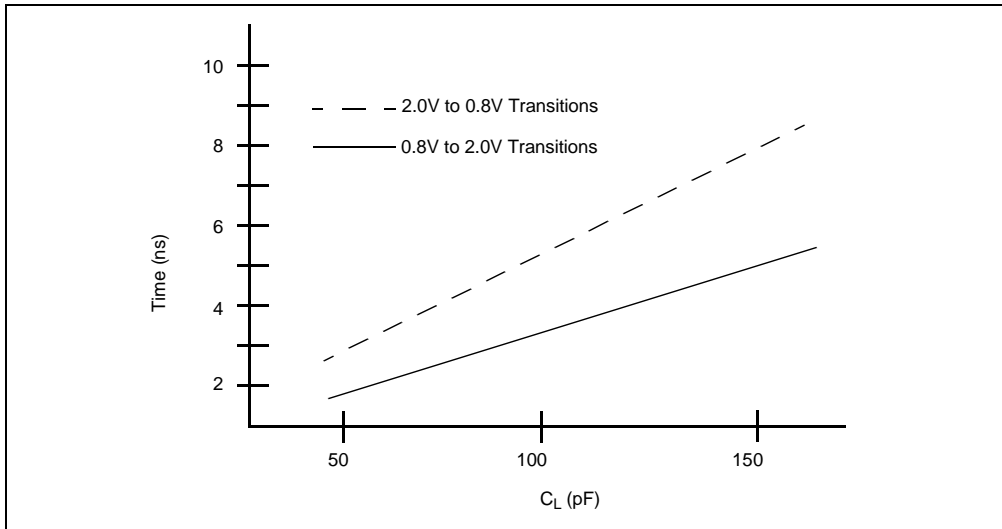


Figure 8. Rise and Fall Time Derating

4.5.2 AC Timing Waveforms

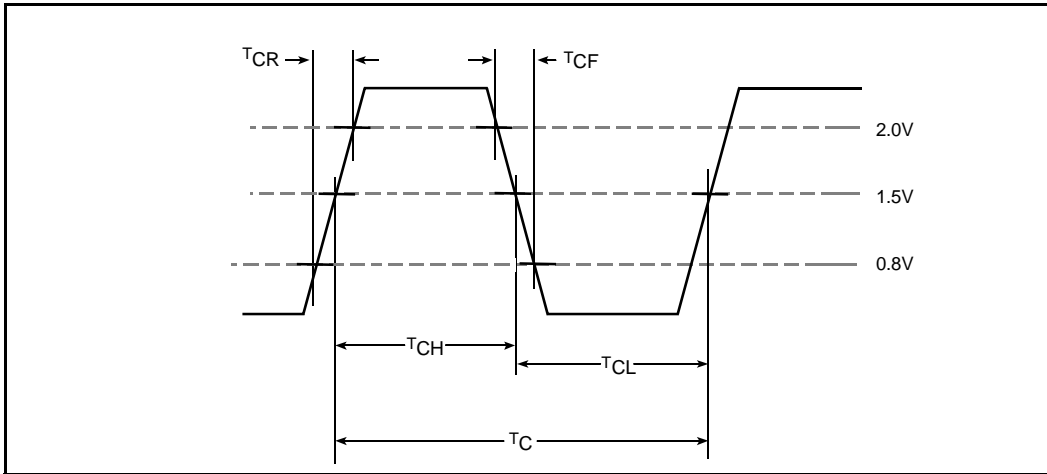


Figure 9. CLKIN Waveform

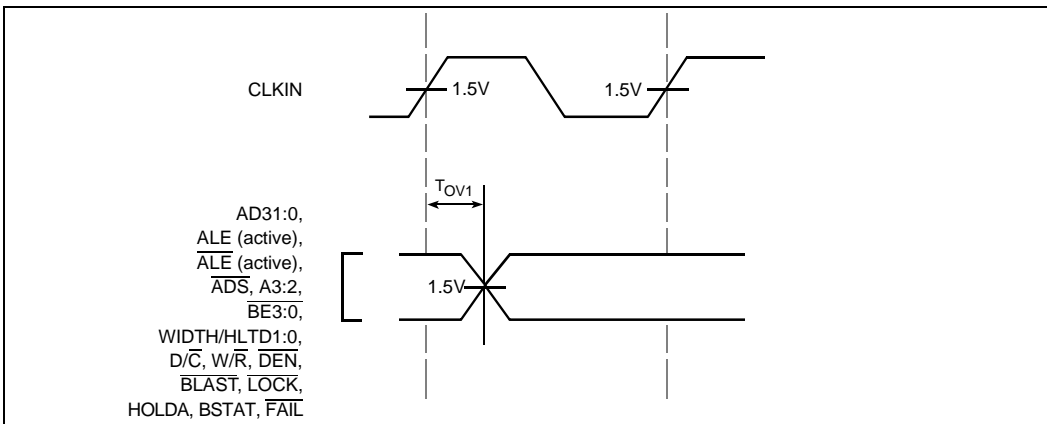


Figure 10. Output Delay Waveform for T_{OV1}

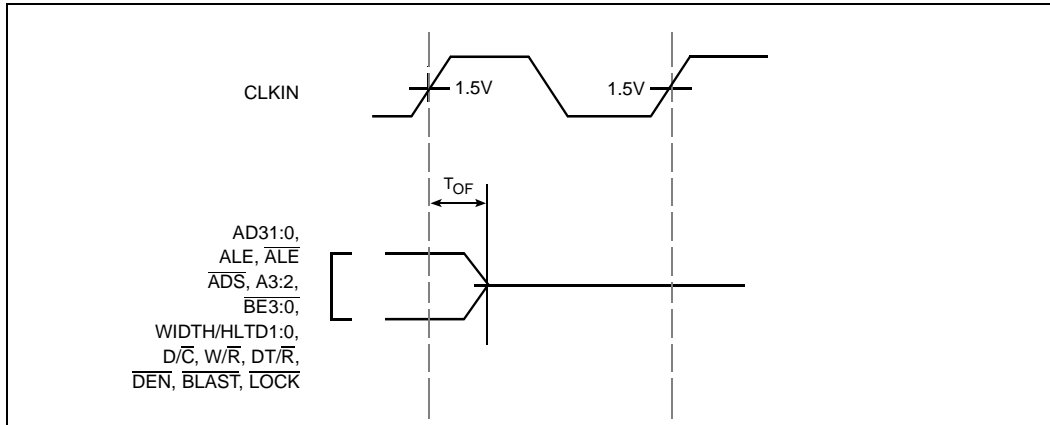


Figure 11. Output Float Waveform for T_{OF}

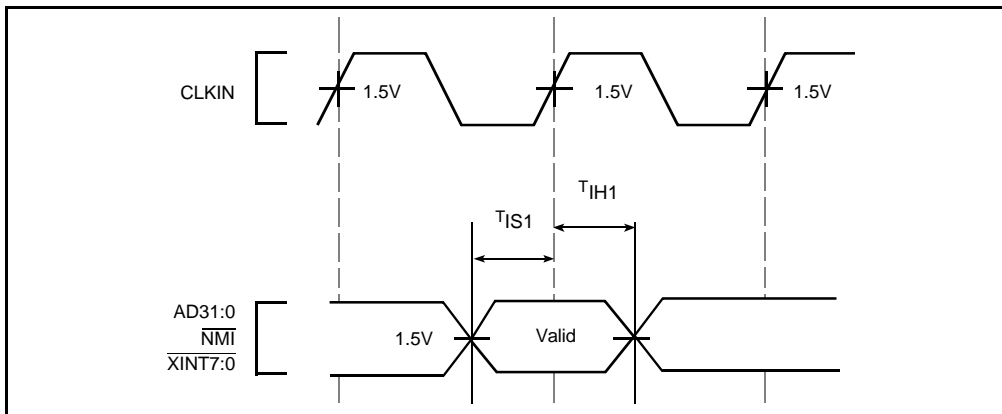


Figure 12. Input Setup and Hold Waveform for T_{IS1} and T_{IH1}

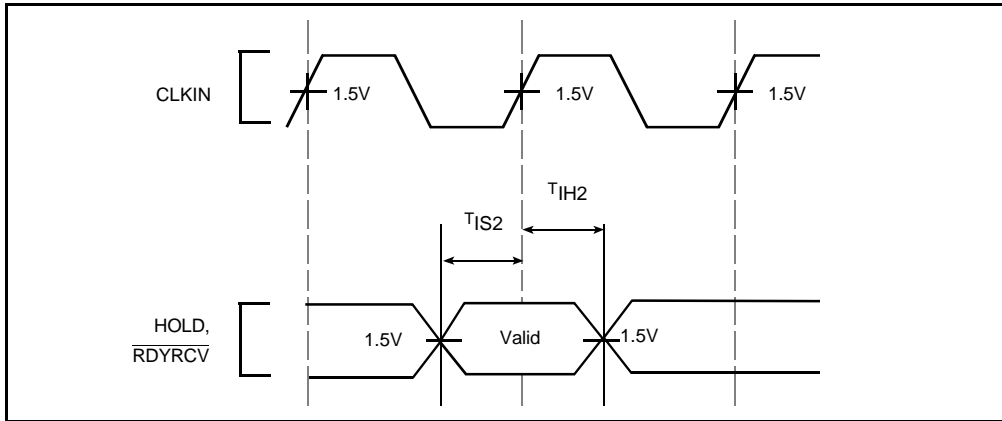


Figure 13. Input Setup and Hold Waveform for T_{IS2} and T_{IH2}

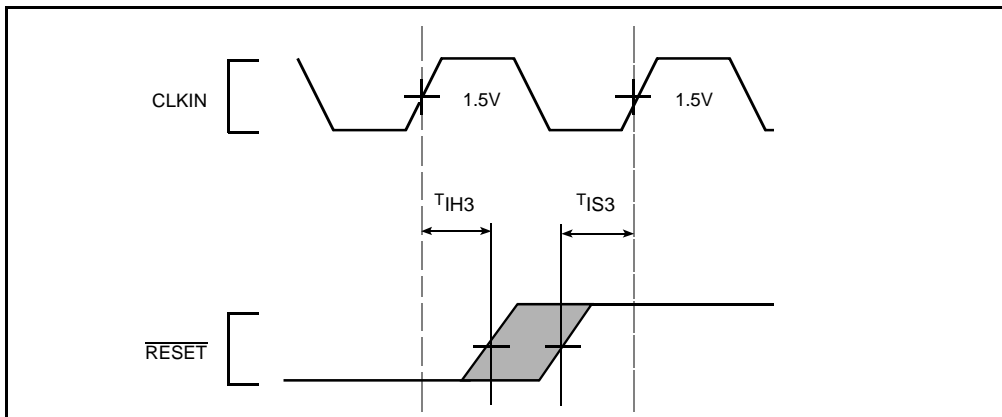


Figure 14. Input Setup and Hold Waveform for T_{IS3} and T_{IH3}

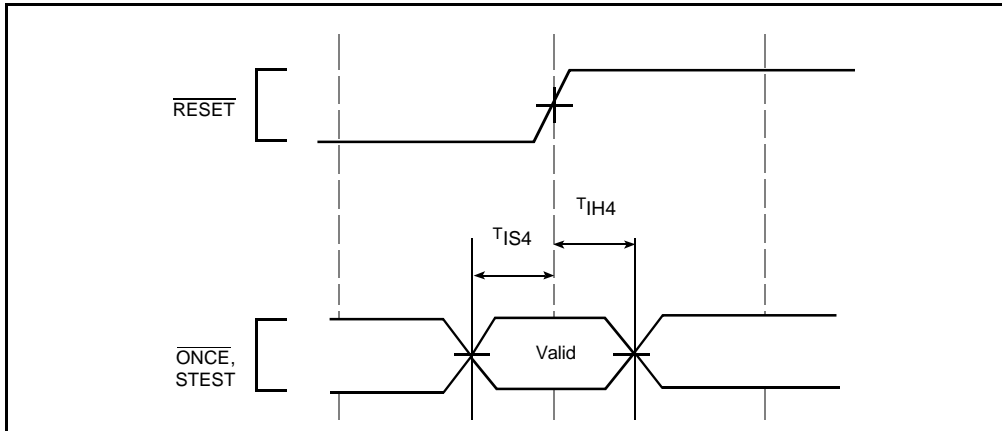


Figure 15. Input Setup and Hold Waveform for T_{IS4} and T_{IH4}

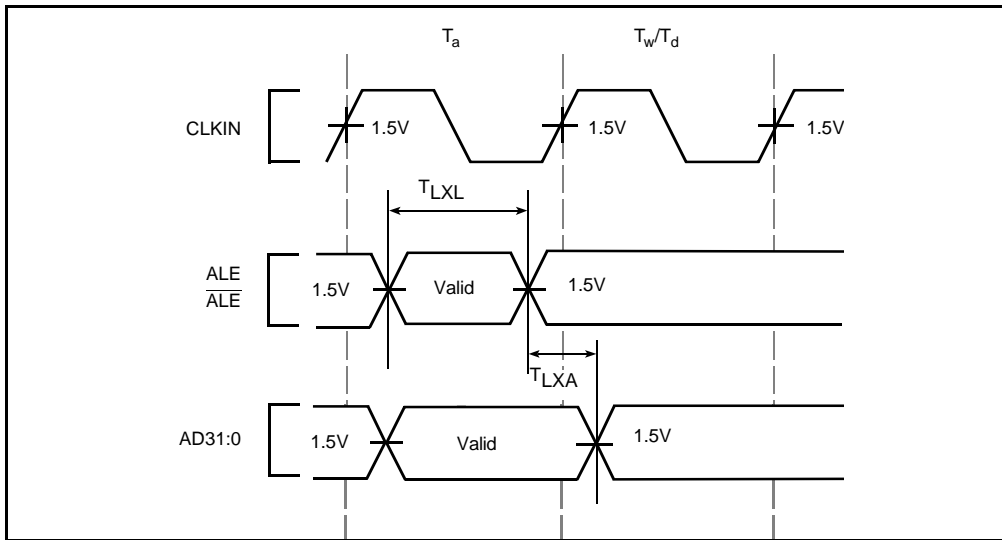


Figure 16. Relative Timings Waveform for T_{LXL} and T_{LXA}

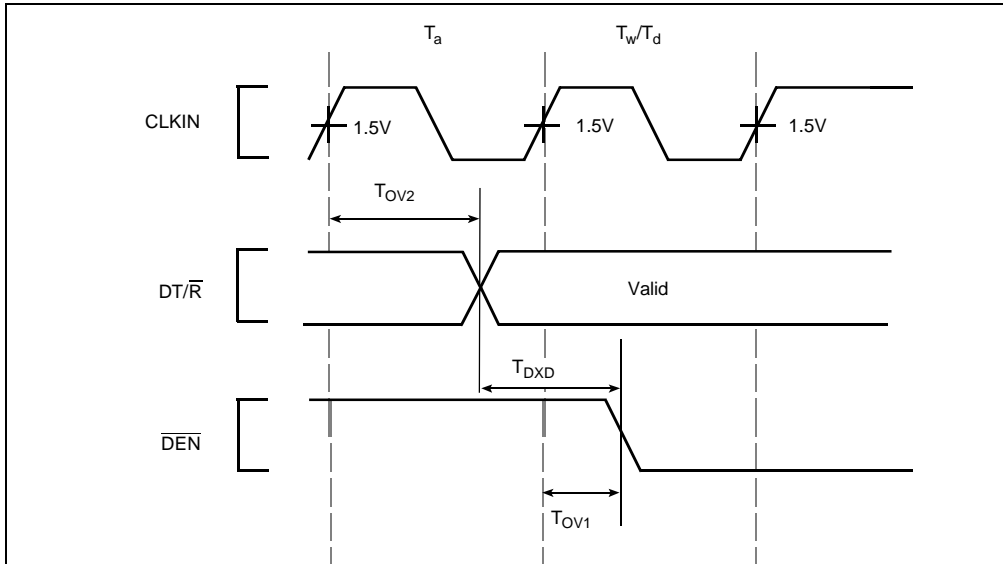


Figure 17. DT/R and DEN Timings Waveform

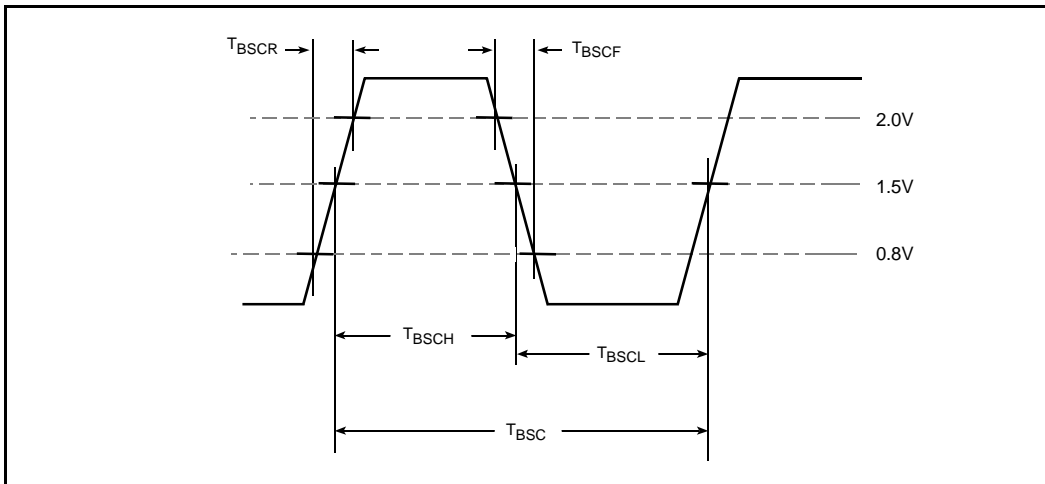


Figure 18. TCK Waveform

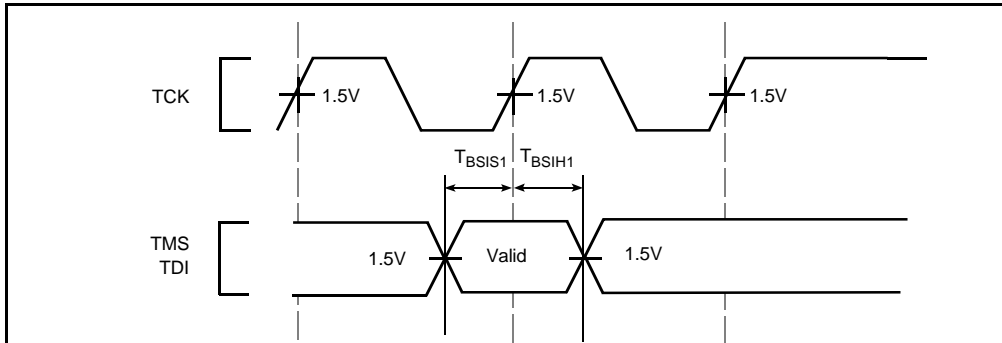


Figure 19. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

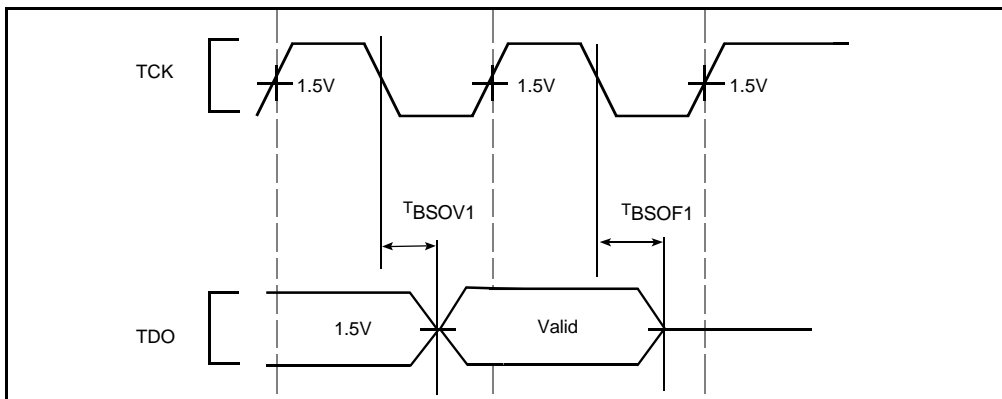


Figure 20. Output Delay and Output Float for T_{BSOV1} AND T_{BSOF1}

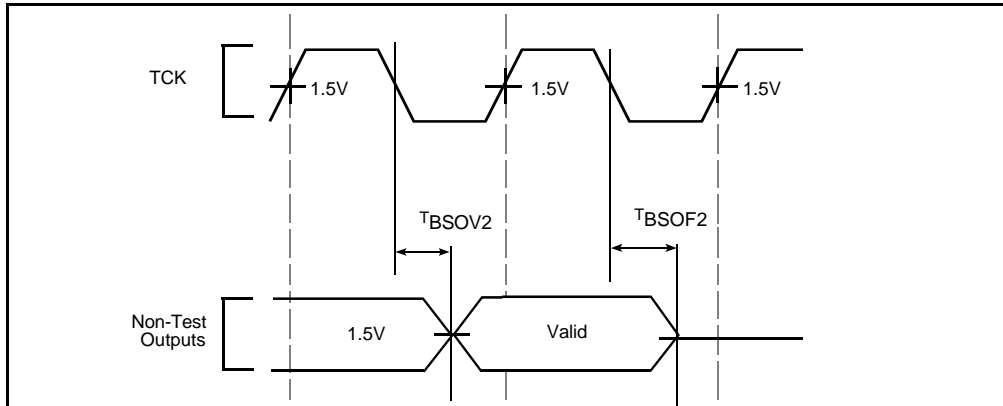


Figure 21. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}

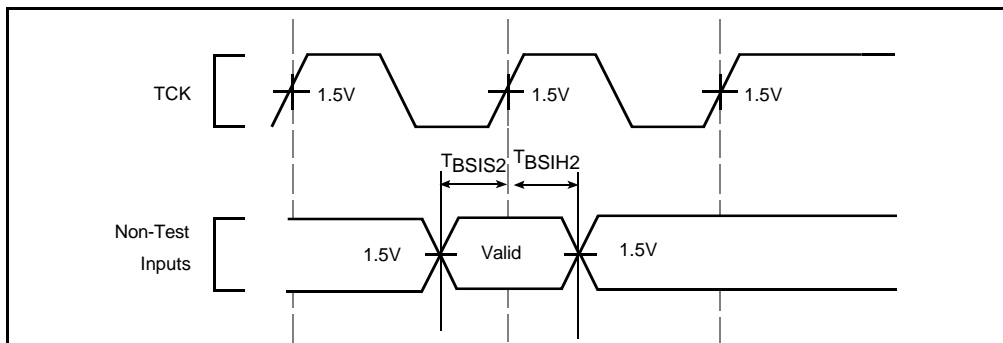


Figure 22. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}

5.0 BUS FUNCTIONAL WAVEFORMS

Figures 23 through 28 illustrate typical 80960JA/JF bus transactions. Figure 29 depicts the bus arbitration sequence. Tables 19 through 22 summarize all possible combinations of bus

accesses across 8-, 16-, and 32-bit buses according to data alignment. Figures 30 and 31 also show accesses on 32-bit buses. Figure 32 illustrates the processor reset sequence from the time power is applied to the device.

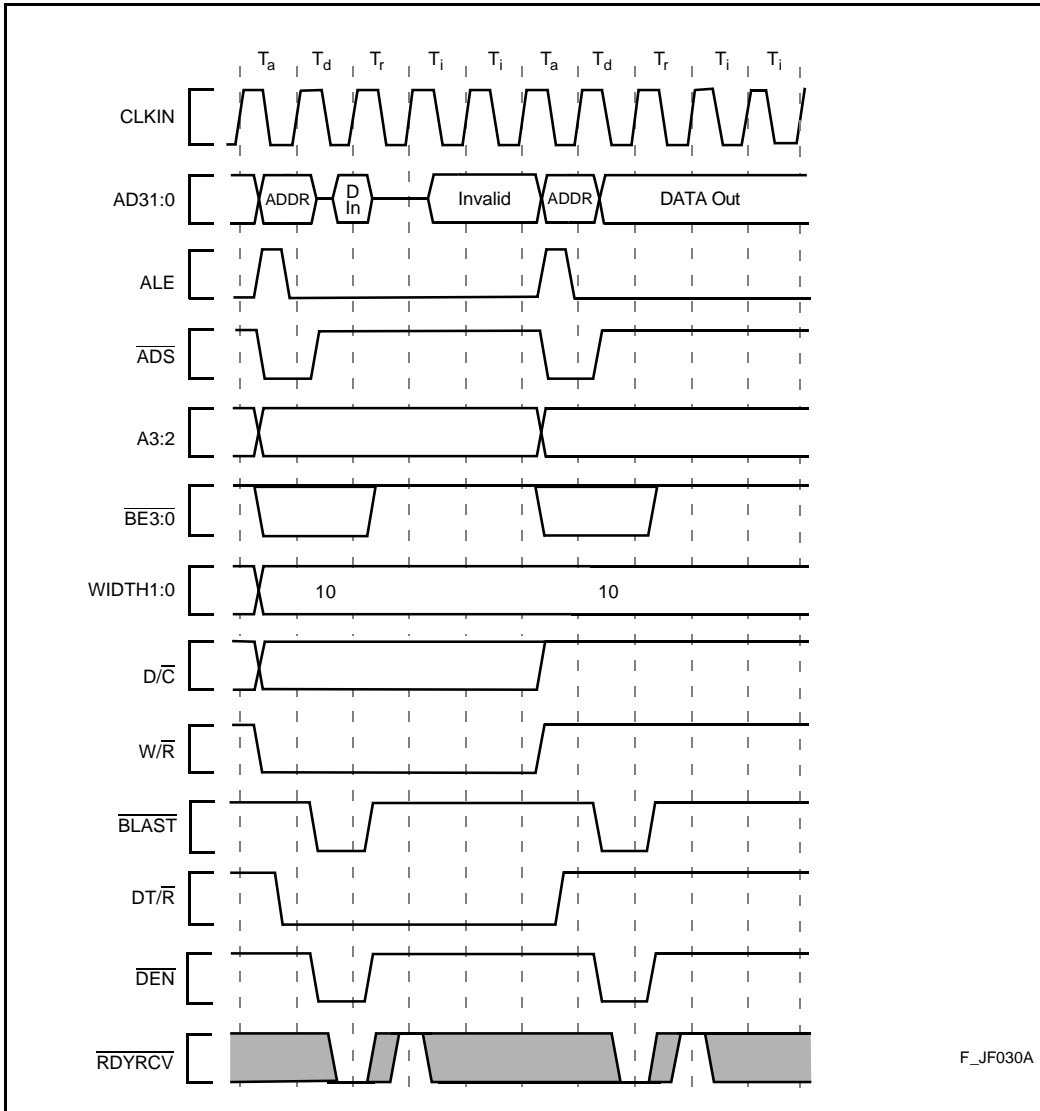


Figure 23. Non-Burst Read and Write Transactions Without Wait States, 32-Bit Bus

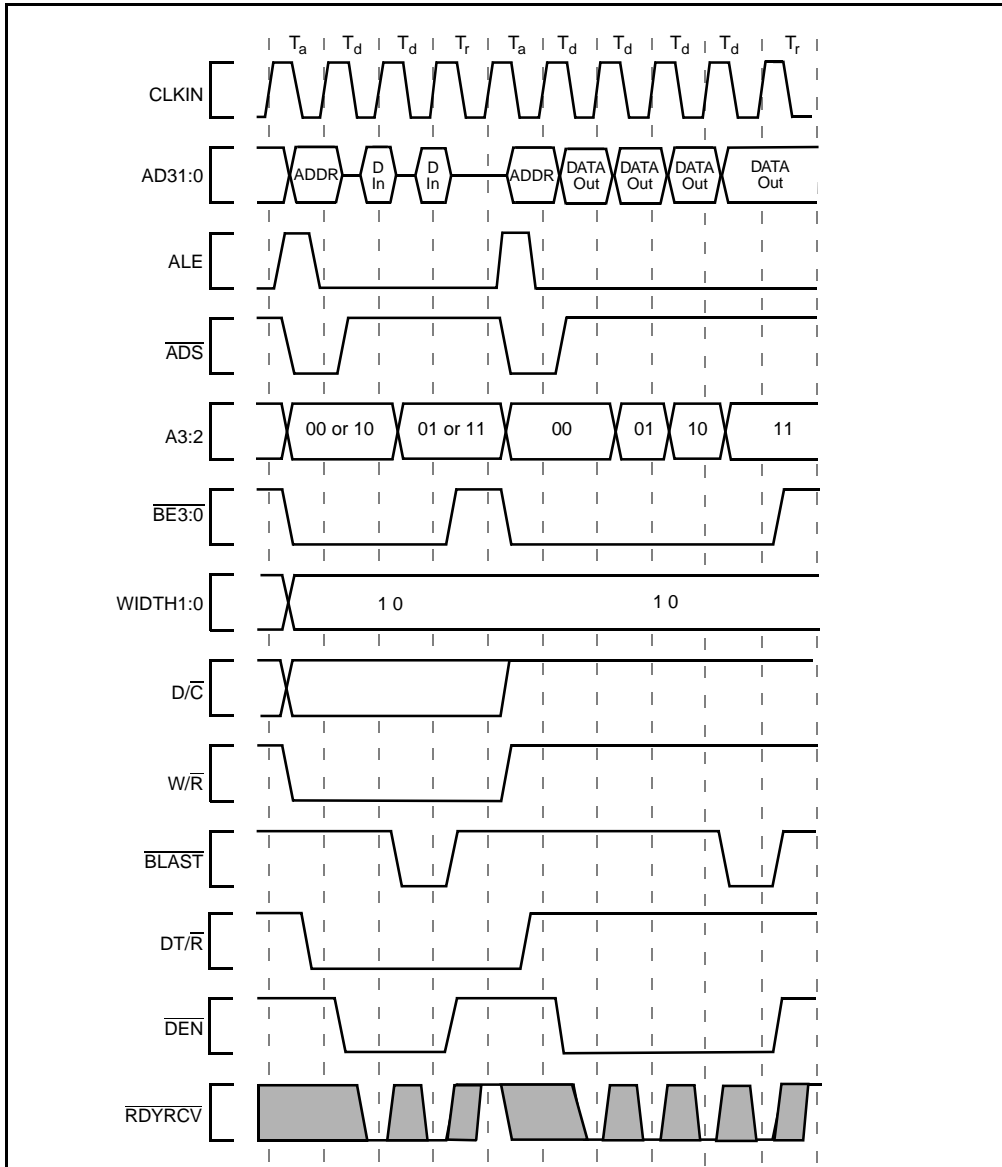


Figure 24. Burst Read and Write Transactions Without Wait States, 32-Bit Bus

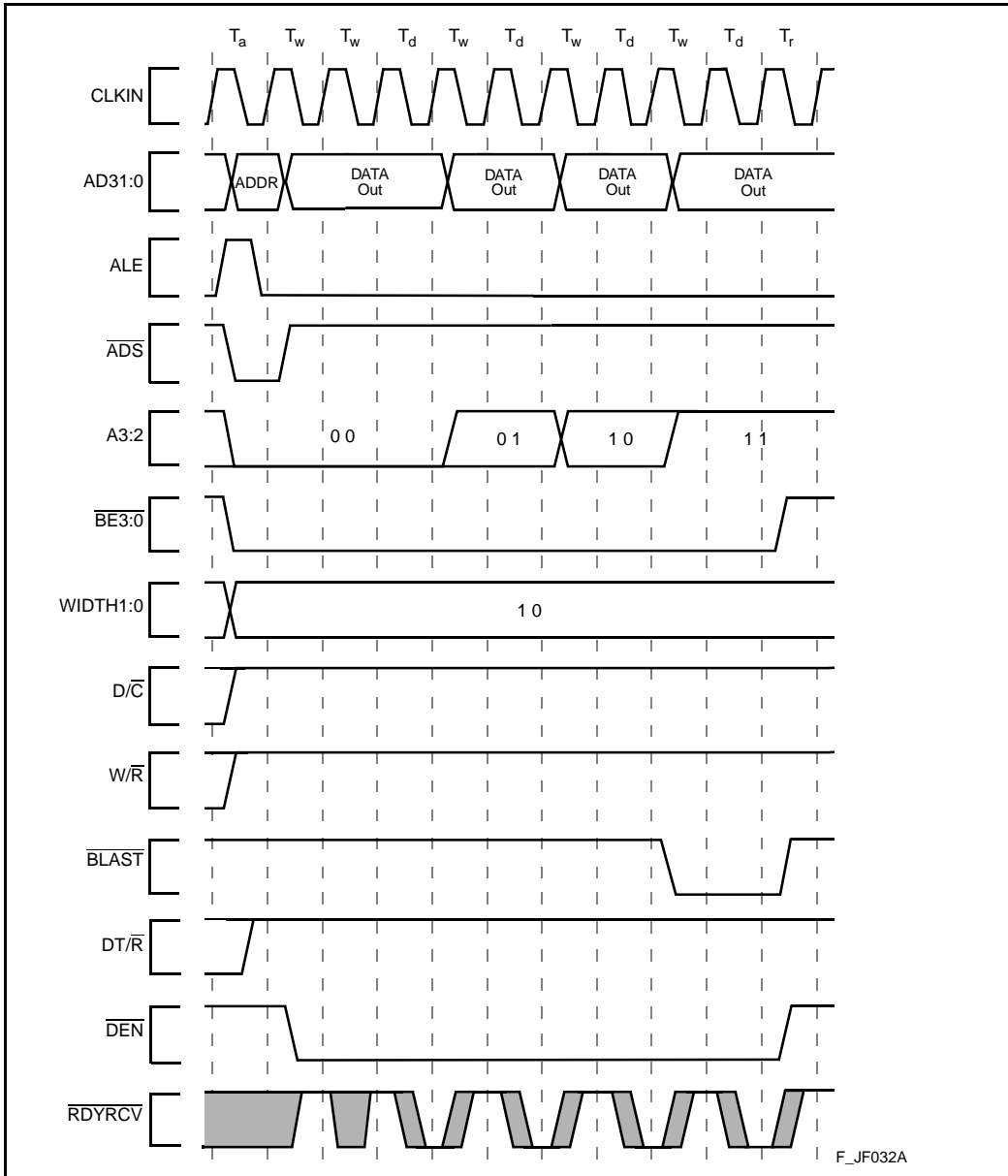


Figure 25. Burst Write Transactions With 2,1,1,1 Wait States, 32-Bit Bus

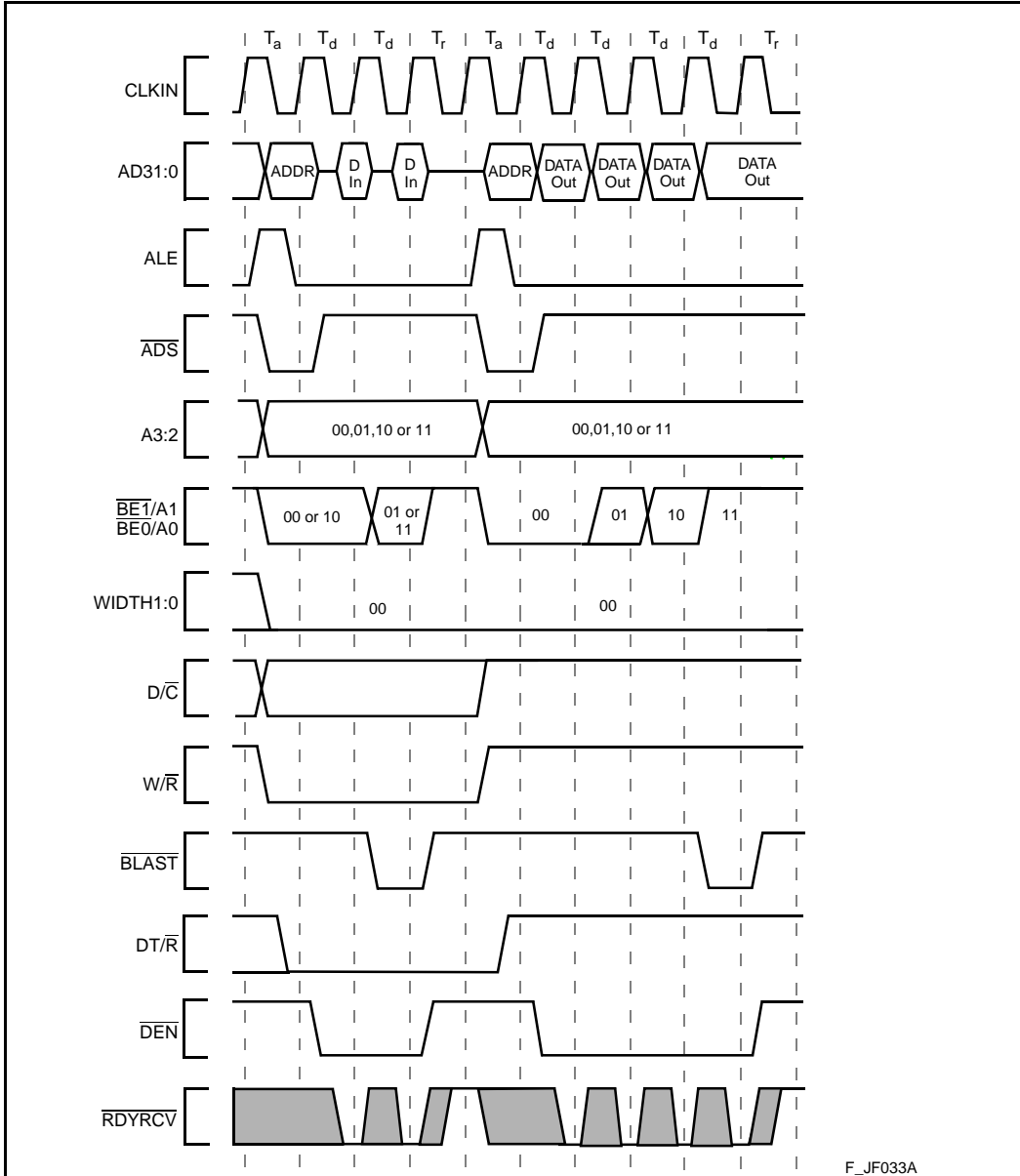
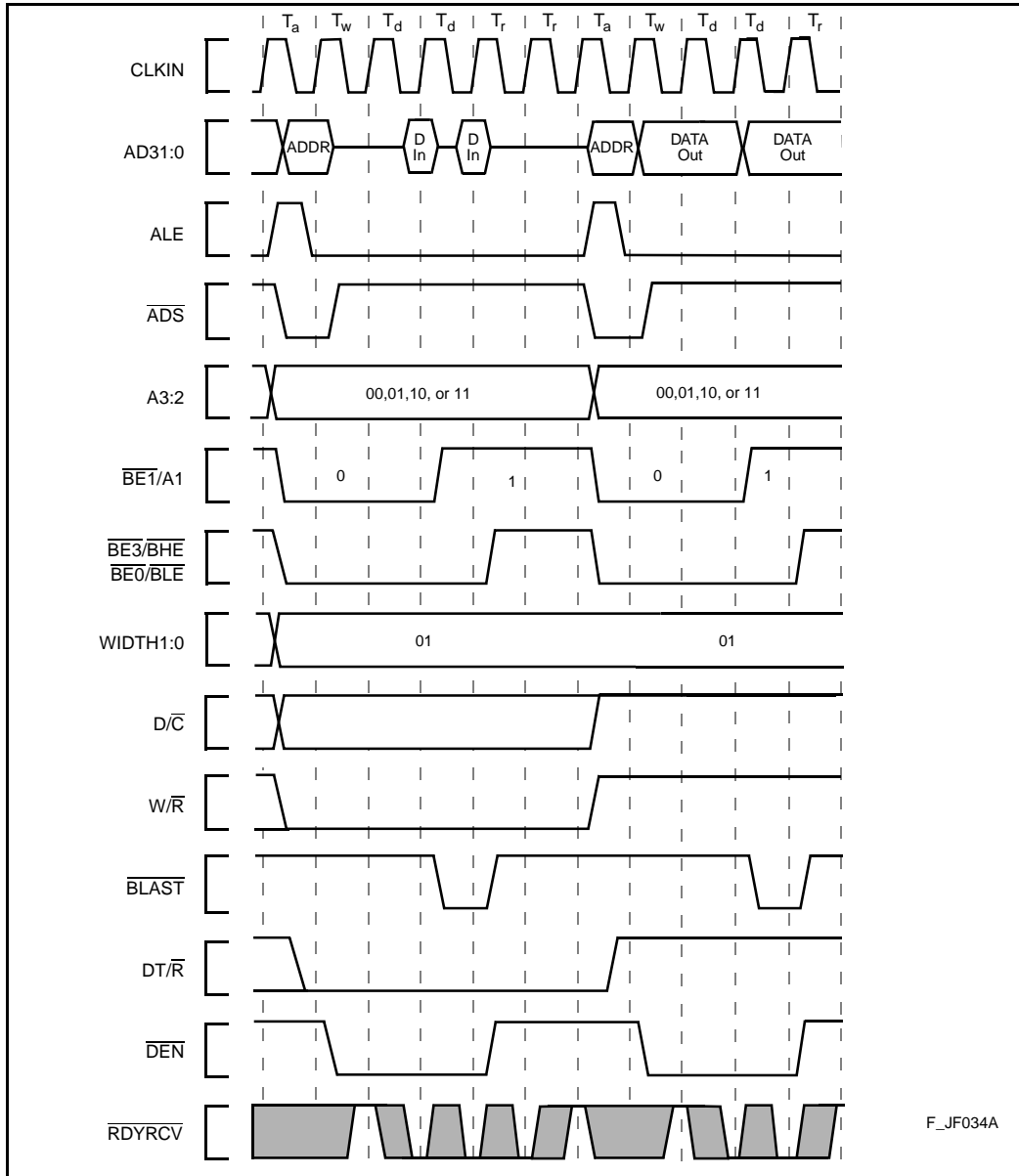


Figure 26. Burst Read and Write Transactions Without Wait States, 8-Bit Bus



F_JF034A

Figure 27. Burst Read and Write Transactions With 1, 0 Wait States and Extra T_r State on Read, 16-Bit Bus

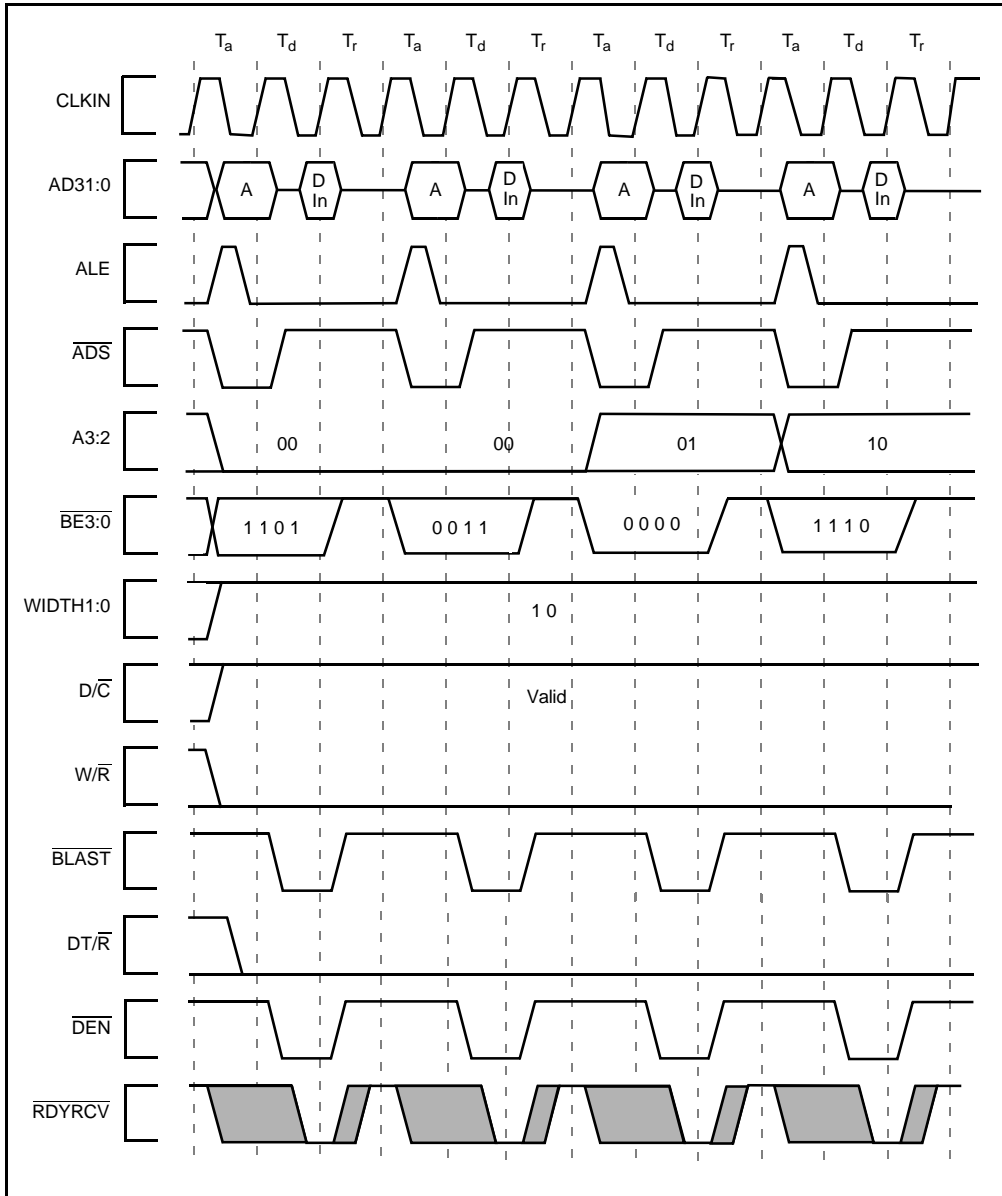


Figure 28. Bus Transactions Generated by Double Word Read Bus Request, Misaligned One Byte From Quad Word Boundary, 32-Bit Bus, Little Endian

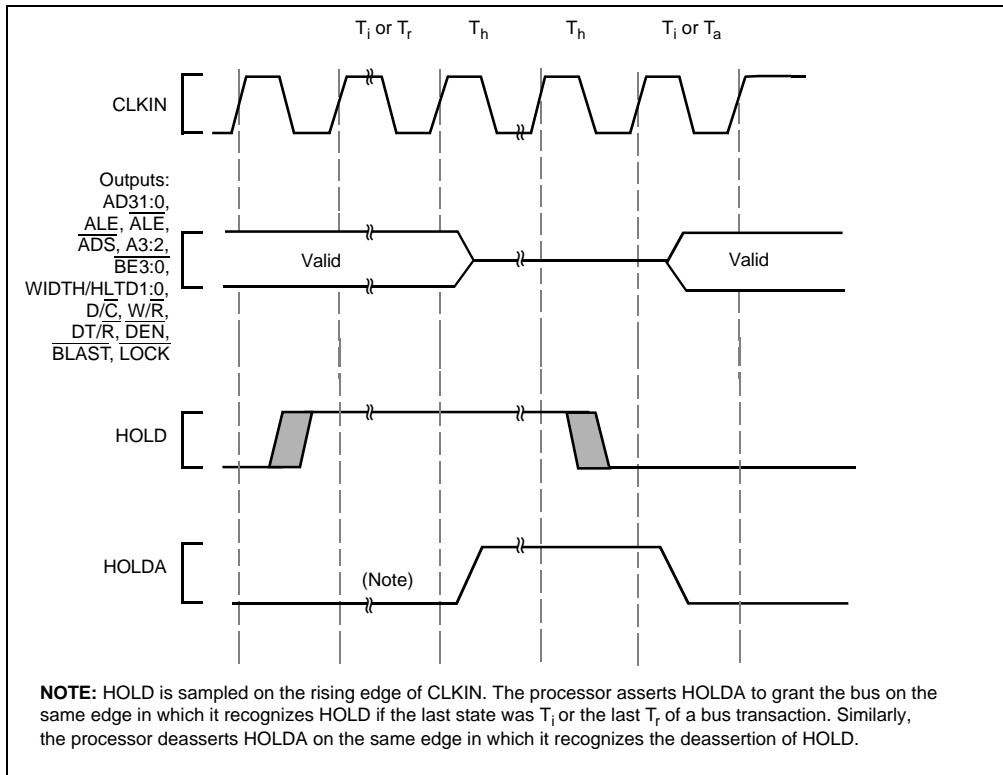


Figure 29. HOLD/HOLDA Waveform For Bus Arbitration

Table 19. Natural Boundaries for Load and Store Accesses

Data Width	Natural Boundary (Bytes)
Byte	1
Short Word	2
Word	4
Double Word	8
Triple Word	16
Quad Word	16

Table 20. Summary of Byte Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• byte access	• byte access	• byte access

Table 21. Summary of Short Word Load and Store Accesses

Address Offset from Natural Boundary (in Bytes)	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned)	• burst of 2 bytes	• short-word access	• short-word access
+1	• 2 byte accesses	• 2 byte accesses	• 2 byte accesses

Table 22. Summary of n -Word Load and Store Accesses ($n = 1, 2, 3, 4$)

Address Offset from Natural Boundary in Bytes	Accesses on 8-Bit Bus (WIDTH1:0=00)	Accesses on 16 Bit Bus (WIDTH1:0=01)	Accesses on 32 Bit Bus (WIDTH1:0=10)
+0 (aligned) ($n = 1, 2, 3, 4$)	• n burst(s) of 4 bytes	<ul style="list-style-type: none"> case $n=1$: burst of 2 short words case $n=2$: burst of 4 short words case $n=3$: burst of 4 short words burst of 2 short words case $n=4$: 2 bursts of 4 short words 	• burst of n word(s)
+1 ($n = 1, 2, 3, 4$) +5 ($n = 2, 3, 4$) +9 ($n = 3, 4$) +13 ($n = 3, 4$)	<ul style="list-style-type: none"> byte access burst of 2 bytes $n-1$ burst(s) of 4 bytes byte access 	<ul style="list-style-type: none"> byte access short-word access $n-1$ burst(s) of 2 short words byte access 	<ul style="list-style-type: none"> byte access short-word access $n-1$ word access(es) byte access
+2 ($n = 1, 2, 3, 4$) +6 ($n = 2, 3, 4$) +10 ($n = 3, 4$) +14 ($n = 3, 4$)	<ul style="list-style-type: none"> burst of 2 bytes $n-1$ burst(s) of 4 bytes burst of 2 bytes 	<ul style="list-style-type: none"> short-word access $n-1$ burst(s) of 2 short words short-word access 	<ul style="list-style-type: none"> short-word access $n-1$ word access(es) short-word access
+3 ($n = 1, 2, 3, 4$) +7 ($n = 2, 3, 4$) +11 ($n = 3, 4$) +15 ($n = 3, 4$)	<ul style="list-style-type: none"> byte access $n-1$ burst(s) of 4 bytes burst of 2 bytes byte access 	<ul style="list-style-type: none"> byte access $n-1$ burst(s) of 2 short words short-word access byte access 	<ul style="list-style-type: none"> byte access $n-1$ word access(es) short-word access byte access
+4 ($n = 2, 3, 4$) +8 ($n = 3, 4$) +12 ($n = 3, 4$)	• n burst(s) of 4 bytes	• n burst(s) of 2 short words	• n word access(es)

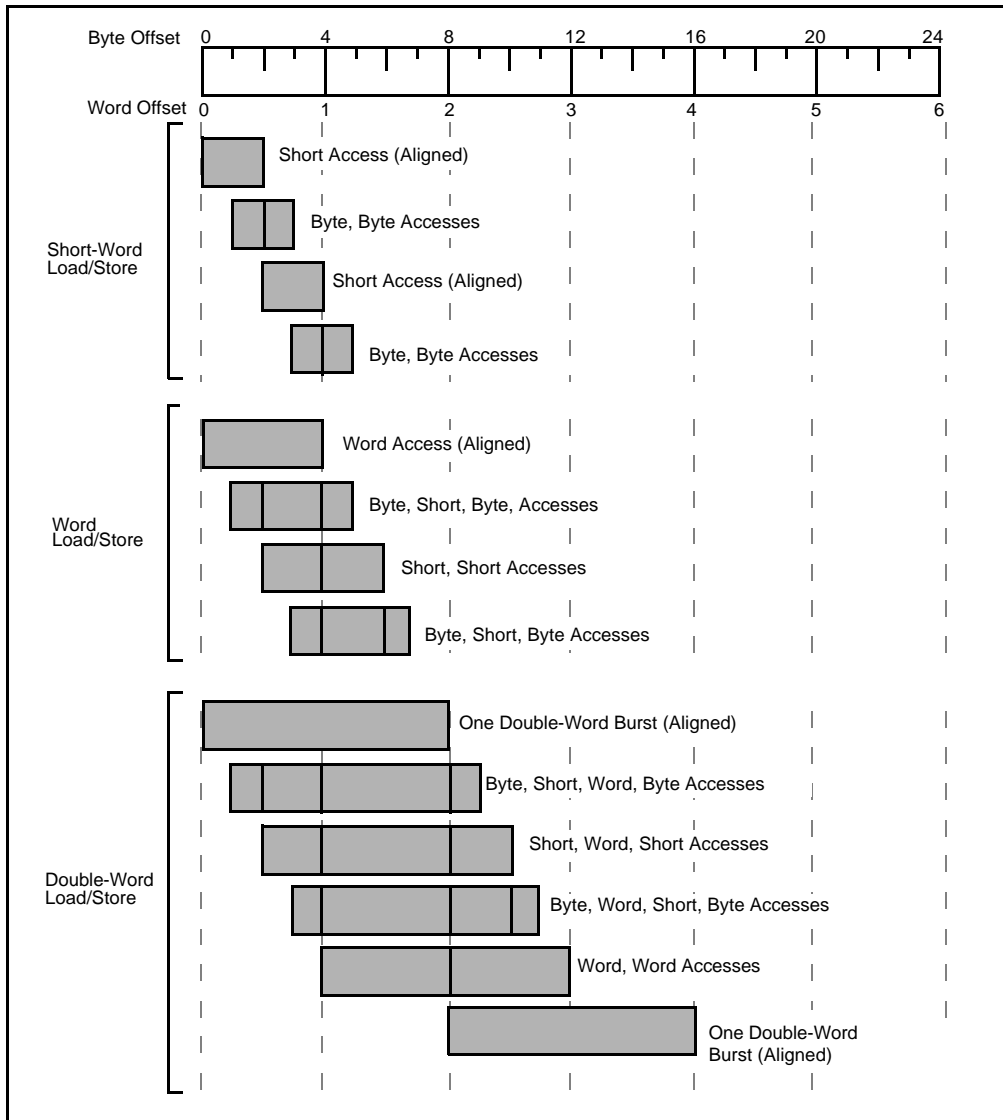


Figure 30. Summary of Aligned and Unaligned Accesses (32-Bit Bus)

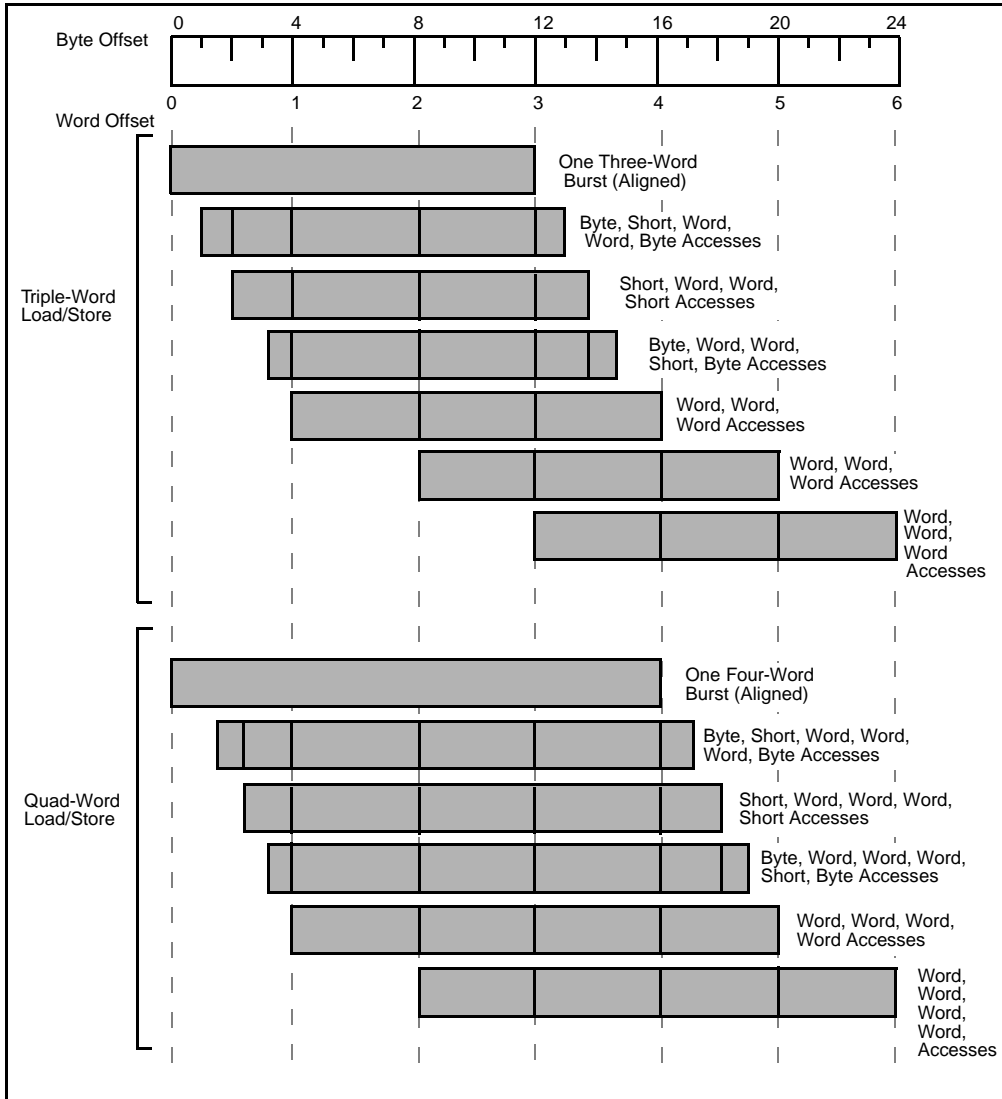
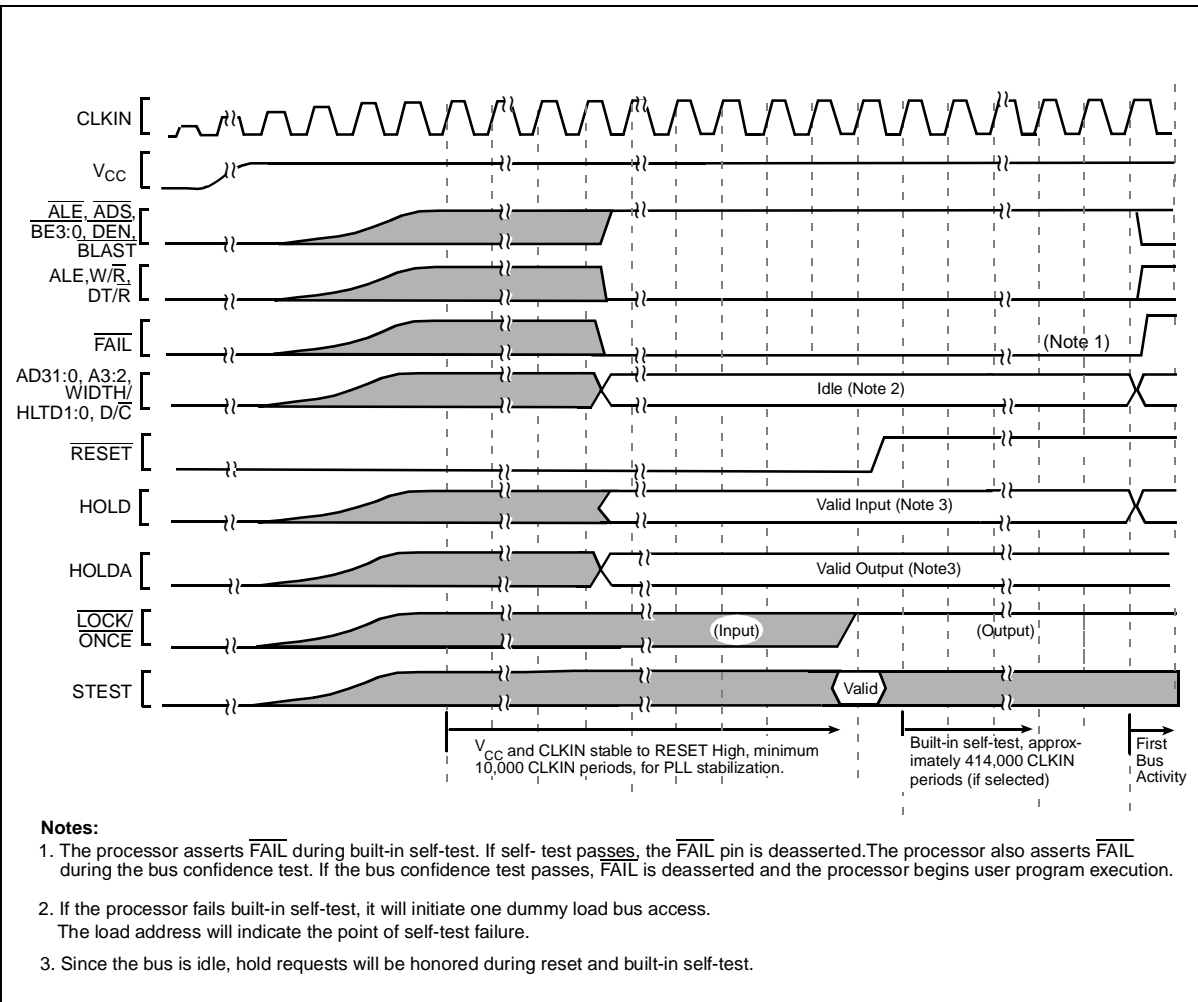


Figure 31. Summary of Aligned and Unaligned Accesses (32-Bit Bus) (Continued)

Figure 32. Cold Reset Waveform



6.0 DEVICE IDENTIFICATION

80960JA/JF processors may be identified electrically according to device type and stepping (see Table 23). The 32-bit identifier is accessible in three ways:

- Upon reset, the identifier is placed into the g0 register.
- The identifier may be accessed from supervisor mode at any time by reading the DEVICEID register at address FF008710H.
- The IEEE Standard 1149.1 Test Access Port may select the DEVICE ID register through the IDCODE instruction.

The stepping number is also printed on the top side of the product package.

Table 23. 80960JA/JF Die and Stepping Reference

Device and Stepping	Version Number	Part Number	Manufacturer	X	Complete ID (Hex)
80960JA A0	0000	1000 1000 0010 0001	0000 0001 001	1	08821013
80960JF A0	0000	1000 1000 0010 0000	0000 0001 001	1	08820013

7.0 REVISION HISTORY

This data sheet supersedes revision 272504-002. Table 24 indicates significant changes since the previous revision.

Table 24. Data Sheet Version -002 to -003 Revision History (Sheet 1 of 2)

Section	Last Rev.	Description
Section 4.3, Connection Recommendations (pg. 21)	-002	Added precaution to drive $\overline{\text{TRST}}$ pin low to reset the TAP controller, even if the JTAG Boundary Scan function will not be used.
Table 13, Targeted 80960JA/JF DC Characteristics (pg. 22)	-002	Changed I_{L1} specification to I_{L11} and added new specification I_{L12} to denote leakage for TAP controller pins. I_{CC} ONCE mode now indicated as 19mA (typ.) and 30 mA (max.).
Table 14, Targeted 80960JA/JF Input Clock Timings (pg. 23)	-002	Minimum CLKIN frequency now specified as 8 MHz.
Table 15, Targeted 80960JA/JF Synchronous Output Timings (pg. 24)	-002	T_{OV1} (min.) improved from 2.5 ns to 3 ns. T_{OV2} (min.) improved from $0.5 T_C + 2.5$ ns to $0.5 T_C + 3$ ns.
Table 16, Targeted 80960JA/JF Synchronous Input Timings (pg. 24)	-002	T_{IS1} and T_{IH1} now applicable to $\overline{\text{NMI}}$ and $\overline{\text{XINT7:0}}$ signals with setup time (min.) improved from 7 to 6 ns and hold time (min.) improved from 3 to 2 ns. T_{IH2} (min.) improved from 2 to 1 ns. T_{IS4} (min.) improved from 7 to 6 ns and T_{IH4} (min.) improved from 3 to 2 ns, with T_{IS4} and T_{IH4} now measured from the inactive edge of $\overline{\text{RESET}}$.
Figure 7, Output Delay or Hold vs. Load Capacitance (pg. 26) Figure 8, Rise and Fall Time Derating (pg. 26)	-002	Inserted data.

Table 24. Data Sheet Version -002 to -003 Revision History (Sheet 2 of 2)

Section	Last Rev.	Description
Figure 12, Input Setup and Hold Waveform for TIS1 and TIH1 (pg. 28) Figure 15, Input Setup and Hold Waveform for TIS4 and TIH4 (pg. 30)	-002	Figures redrawn to correspond to changes in setup and hold specifications for NMI, XINT7:0, ONCE and STEST.

Table 24 indicates significant changes between revisions -001 and -002.

Table 25. Data Sheet Version -001 to -002 Revision History (Sheet 1 of 2)

Section	Last Rev.	Description
Figure 2, 80960JA/JF Block Diagram (pg. 2)	-001	Added 80960JA product version, which includes 2 Kbyte instruction cache and 1 Kbyte data cache.
Table 1, 80960JA/JF Instruction Set (pg. 5)	-001	Renamed Conditional Move instruction to Conditional Select instruction.
Table 3, Pin Description — External Bus Signals (pg. 7)	-001	Clarified description of unused AD31:0 pins during write operations. Corrected description of AD31:0 pins during HALT mode. Renamed ADS pin from Address/Data Status to Address Strobe (pin function unchanged). Corrected description of BE3:2 pins to indicate high state when pin(s) unused.
Table 4, Pin Description — Processor Control Signals, Test Signals and Power (pg. 10)	-001	Added note that TDO does not float during ONCE Mode. Added note to ground TRST if TAP unused.
Figure 3, 132-Lead Pin Grid Array Bottom View - Pins Facing Up (pg. 12) Figure 4, 132-Lead Pin Grid Array Top View - Pins Facing Down (pg. 13) Table 6, 132-Lead PGA Pinout — In Signal Order (pg. 14) Table 7, 132-Lead PGA Pinout — In Pin Order (pg. 15)	-001	New figures and tables. Pin C8 changed from V_{CC} (previously published elsewhere) to NC. Processor operates correctly in a system with either connection.
Figure 5, 132-Lead PQFP - Top View (pg. 16) Table 8, 132-Lead PQFP Pinout — In Signal Order (pg. 17) Table 9, 132-Lead PQFP Pinout — In Pin Order (pg. 18)	-001	New figure and tables. Lead 19 changed from $V_{CC(I/O)}$ (previously published elsewhere) to NC. Processor operates correctly in a system with either connection.
Section 3.2, Package Thermal Specifications (pg. 19)	-001	New section with tables of thermal characteristics.
Section 4.0, ELECTRICAL SPECIFICATIONS (pg. 21)	-001	New section with targeted operating conditions, targeted DC characteristics, targeted AC specifications and AC timing waveforms.
Figure 29, HOLD/HOLDA Waveform For Bus Arbitration (pg. 40)	-001	Improved figure.

Table 25. Data Sheet Version -001 to -002 Revision History (Sheet 2 of 2)

Section	Last Rev.	Description
Table 19, Natural Boundaries for Load and Store Accesses (pg. 40) Table 20, Summary of Byte Load and Store Accesses (pg. 41) Table 21, Summary of Short Word Load and Store Accesses (pg. 41) Table 22, Summary of n-Word Load and Store Accesses (n = 1, 2, 3, 4) (pg. 41) Figure 30, Summary of Aligned and Unaligned Accesses (32-Bit Bus) (pg. 42)	-001	New tables and figures to explain bus access alignment.
Figure 32, Cold Reset Waveform (pg. 44)	-001	New figure.
Section 6.0, DEVICE IDENTIFICATION (pg. 45)	-001	New section.